PhD Thesis

STUDY AND DESIGN OF CMOS RF POWER CIRCUITS AND MODULATION CAPABILITIES FOR COMMUNICATION APPLICATIONS

Heider Marcôni Guedes Madureira

Brasilia, June 2015

UNIVERSIDADE DE BRASILIA

FACULDADE DE TECNOLOGIA

UNIVERSIDADE DE BRASÍLIA
FACULDADE DE TECNOLOGIA

STUDY AND DESIGN OF CMOS RF POWER CIRCUITS AND MODULATION CAPABILITIES FOR COMMUNICATIONS APPLICATIONS

HEIDER MARCONI GUEDES MADUREIRA

ORIENTADORA: SANDRO AUGUSTO PAVLIK HADDAD

TESE DE DOUTORADO EM ENGENHARIA ELÉTRICA

PUBLICAÇÃO: PGEA.TD – 095/2015

BRASÍLIA/DF: JUNHO – 2015

UNIVERSIDADE DE BRASÍLIA
FACULDADE DE TECNOLOGIA
DEPARTAMENTO DE ENGENHARIA ELÉTRICA

STUDY AND DESIGN OF CMOS POWER CIRCUITS AND MODULATION CAPABILITIES FOR COMMUNICATION APPLICATIONS

HEIDER MARCONI GUEDES MADUREIRA

TESE DE DOUTORADO SUBMETIDA AO DEPARTAMENTO DE ENGENHARIA ELÉTRICA DA FACULDADE DE TECNOLOGIA DA UNIVERSIDADE DE BRASÍLIA, COMO PARTE DOS REQUISITOS NECESSÁRIOS PARA A OBTENÇÃO DO GRAU DE DOUTOR.

APROVADA POR:

SANDRO AUGUSTO PAVLIK HADDAD, Dr., FGA/UNB
(ORIENTADOR)

PAULO HENRIQUE PORTELA DE CARVALHO, Dr., ENE/UNB
(EXAMINADOR INTERNO)

ERIC KERHERVÉ, Dr., BORDEAUX
(EXAMINADOR EXTERNO)

ROBSON NUNES DE LIMA, Dr., UFBA
(EXAMINADOR EXTERNO)

ANDRÉ AUGUSTO MARIANO, Dr., UFPR
(EXAMINADOR EXTERNO)

ANTONIO AUGUSTO LISBOA DE SOUZA, Dr., UFPB
(EXAMINADOR EXTERNO)

Brasília, 15 de junho de 2015.

FICHA CATALOGRÁFICA

MADUREIRA, HEIDER MARCONI GUEDES

Study and Design of CMOS RF Power Circuits and Modulation Capabilities for Communication Applications [Distrito Federal] 2015.

vii, 86p., 210 x 297 mm (PGEA/ENE/FT/UnB, Doutor, Tese de Doutorado – Universidade de Brasília. Faculdade de Tecnologia.

Departamento de Engenharia Elétrica

1.Oscilador de potência 2.Amplificador de potência

3.CMOS 4.Radiofrequência

I. ENE/FT/UnB II. Título (série)

REFERÊNCIA BIBLIOGRÁFICA

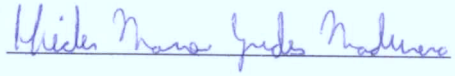
MADUREIRA, H. M. G (2015). Study and Design of CMOS RF Power Circuits and Modulation Capabilities for Communication Applications. Tese de doutorado em Engenharia Elétrica, Publicação PGEA.TD - 095/2015, Departamento de Engenharia Elétrica, Universidade de Brasília, Brasília, DF, 86p.

CESSÃO DE DIREITOS

AUTOR: Heider Marconi Guedes Madureira.

TÍTULO: Study and Design of CMOS RF Power Circuits and Modulation Capabilities for Communications Applications.

GRAU: Doutor ANO: 2015



Heider Marconi Guedes Madureira
SQS 410 Bloco Q Apt 201B
70.276-170 Brasília – DF – Brasil.

Dedicatória

A todos que eu chamo de família. E aos que sonharam com isso.

Heider Marcôni Guedes Madureira

Acknowledgements

Gostaria de agradecer meus orientadores Sandro Haddad, Nathalie Deltimple e Eric Kerhervé pelo trabalho e dedicação. Aos Professores José Camargo da Costa e Paulo Henrique Portela pela oportunidade que me foi dada de ser parte do time e morar na França. A todos os meus amigos pela força e ajuda em momentos de muito trabalho e as vezes nem tanto. Gostaria de agradecer o amigos Marcos Carneiro, Dean Karolak, Rosário Desposito, Mario Weiss, Oskar Holstensson e Dwight Cabrera pela convivência e trabalho compartilhado. Ao time da DFchip, em especial ao amigo Rafael Ferreira, por segurar quando precisei me ausentar. Ao velho time do LPCI, José Edil, Gilmar Beserra, Genival Araújo, Daniel Café, Pedro Aurélio pela convivência que culminou neste trabalho. À amiga Ana Régia Neves pela força e incentivos incansáveis. Finalmente desejo agradecer minha mãe, Wany de Cassia de Carvalho Guedes, e meu pai, Marco Aurélio Madureira Ribeiro, por absolutamente TUDO. Este trabalho é apenas uma ínfima parte do que seria impossível sem o apoio de vocês.

Heider Marcôni Guedes Madureira

ABSTRACT

This work presents the study, design and measurement of RF circuits aiming communications applications. The need for flexible and reconfigurable RF hardware leads to the need of alternative transmitter architectures. In the center of this innovative architecture, there is the power oscillator. This circuit is composed of a power amplifier in a positive feedback loop so it oscillates. As the circuit under study is mainly composed of a power amplifier, a study on power amplifier is mandatory. Modern CMOS technologies impose difficulties in the efficient RF generation due to low breakdown voltages. In order to reduce the voltage stress on the transistors, waveform engineering techniques are used leading to the use of class EF2. The design and measurement of a class EF2 power amplifier and power oscillator are shown. The circuits were implemented in standard STMICROLECTRONICS 0.13μm CMOS. Correct behavior for the circuits were obtained in measurement, leading to a first implementation of class EF2 in RF frequencies. From a system perspective, the proposed architecture is shown to be flexible and able to generate different modulations without change in the hardware. Reconfigurability is shown not only in modulation but also in output power level. The limitations of this architecture are discussed and some mathematical modeling is presented.

RESUMÉ

Dans lère des systèmes de communication multi-standards, le besoin des circuits en radio fréquence (RF) flexibles et réconfigurables pousse l'industrie et l'academie à la recherche d'architectures alternatives d'émetteurs et récepteurs RF. Dans cette thèse, nous nous intéréssons aux émetteurs RF fléxibles. Nous présentons une architecture basée sur l'utilisation d'un oscillateur de puissance composé dt'un amplificateur de puissance dans une boucle de rétroaction positive. Pour des raisons de compatibilité avec des circuit numériques et dans le but de minimiser les coûts de fabrication, nous avons choisi la technologie CMOS. Ce choix impose des difficultés de concéption de circuits en RF à cause des faibles tensions de claquage. Cette contrainte de concéption nous a motivé à choisir la classe EF2 pour l'amplificateur de puissance afin de réduire le stress de tension sur les transistors. Nous présentons la concéption de cet amplificateur de puissance de classe EF2 ainsi que l'oscilateur de puissance. Nous validons cette architecture avec une implémentation en technologie CMOS 0.13um de STMicroelectronics. Nous démontrons le bon comportement par mesure et tests du circuit fabriqué. Ce circuit répond aux contraintes de fléxibilité de modulation et de puissance de sortie pouvant donc être utilisée pour différents standards de communications. Les limitations inhérentes de cette architecture sont discutées et une modélisation mathématique est présentée.

SUMMARY

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

Symbols

$\mathcal{L}\{\Delta\omega\}$	Phase noise	dBc/Hz

Abbreviations

AM	Amplitude Modulation
FM	Frequency Modulation
PM	Phase Modulation
CAD	Computer Assisted Design
CCO	Current Controlled Oscillator
CMOS	Complementary Metal-Oxide Semiconductor
DRC	Design Rule Check
PCB	Printed Circuit Board
PLL	Phase Locked Loop
DE	Drain Efficiency
PAE	Power Added Efficiency
LNA	Low Noise Amplifier
LVS	Layout versus Schematic
MIM	Metal-Insulator-Metal capacitor
MOM	Metal-Oxide-Metal capacitor
ng	Number of gates
PA	Power Amplifier
PVCO	Power VCO
PD	Phase Detector
PLL	Phase Locked Loop
PNOISE	Periodic Noise
PSS	Periodic Steady State
Q	Quality Factor
RF	Radio Frequency
SoC	System on Chip
VCO	Voltage Controlled Oscillator
VHDL	VHSIC Hardware Description Language

1 INTRODUCTION

1.1 CONTEXTUALIZATION

Energy consumption has become a key aspect in modern electronics. In consumer products such as cell phones and tablets the raising complexity has the goal to offer high computational power and multi-standard communication interfaces. Modern CMOS technology have evolved such that the hardware is very power efficient enabling computational power in portable devices to be comparable to computers. In the context of communication, the use of an optimized circuit for each communication standard increases the battery lifetime but increases the complexity of the PCB as more chips must be placed and connected to the antenna or antennas. RF simulations are often needed to ensure the correct high frequency characteristics of the PCB, increasing development time and cost.

Another application where energy consumption is a key aspect are wireless sensor networks. It is well known that energy is the strongest limitation of these engineering solutions and much work has been presented in order to address this issue, from hardware design [1], efficient communication protocols [2], high level modeling for energy optimization [3] among many others. In this type of application, the communication is also responsible for the largest part of the consumption.

Observing these engineering solutions, it is possible to conclude that, in order to increase the battery lifetime, special care must be taken with the RF transceivers, from hardware to software. In hardware level, the most power hungry circuit inside the transceiver is the power amplifier that is often narrow band and optimized for a given communication standard offering reasonable efficiency. These considerations are made assuming that typical transmitter architectures are used.

The most common architectures are homodyne and heterodyne, discussed in Chapter 2. These systems are based on large number of RF blocks such as filters, mixers and tuned amplifiers. A typical heterodyne transmitter is shown in Figure 1.1.

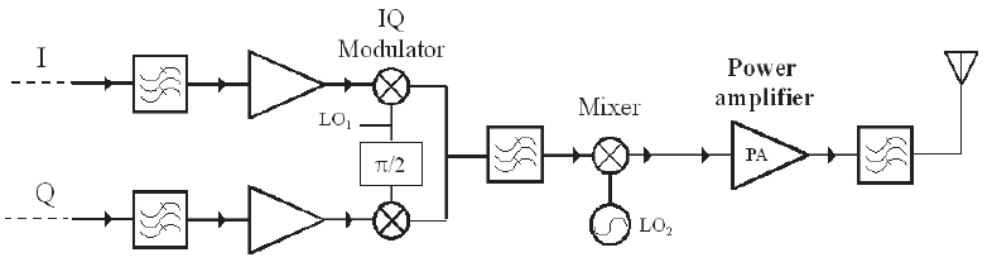


Figure 1.1: Heterodyne transmitter architecture. [4]

Efforts have been made to merge essential RF functions and examples of this trend is shown in [5] [6]. In all these works, the power amplifier is clearly separate from the other circuits. One other trend in architectural level is to simplify the RF part of the transmitter towards digital circuits and the up-conversion as close as possible from the antenna. A simplified RF transmitter is shown in Figure 1.2.

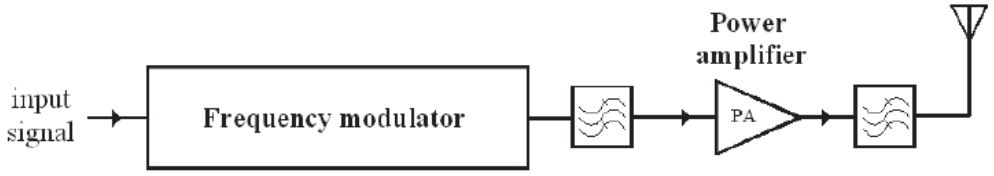


Figure 1.2: Direct modulation architecture [4]

Taking both trends into account, circuit level and architecture level, it is possible to think of a transmitter composed basically by a power oscillator. The modulation of this transmitter is composed of digital or baseband signals that are used to modulate signal generated by the circuit. The proposed architecture is shown in Figure 1.3. The idea is that the input signal modulates the RF carrier. In this way, being able to reconfigure the input signal would lead to a reconfigurable RF transmitter reducing the problems already described for classical architectures.

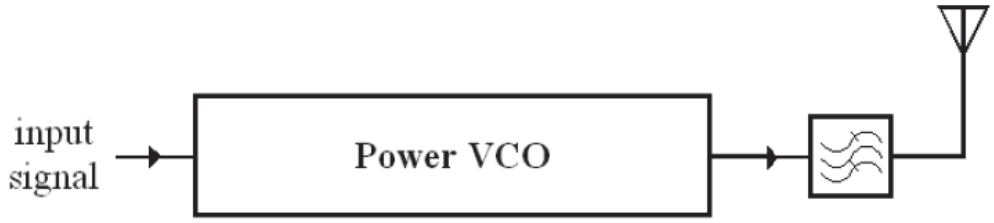


Figure 1.3: Transmitter based on Power Oscillator [4]

Being the center of the whole transmitter it is important to fully understand the characteristics of the power oscillator as well advantages, limitations and difficulties in its design. This work is aimed at this target.

This work is part of a cooperation between University of Brasília and University of Bordeaux implemented in 2010 by a Capes-Cofecub Program coordinated by Professor Paulo Henrique Portela. Two thesis in co-supervision have been supported by the program:

1. The research about the implementation of Doherty power amplifiers in submicron CMOS technologies developed by Marcos Lajovic Carneiro supervised by Professor Paulo Henrique Portela from University of Brasilia, Professor Eric Kerhervé and Associate Professor Nathalie Deltimple from University of Bordeaux and defended in December 2013.

2. This work on the study of power oscillators supervised by Professor Sandro Augusto Pavlik Haddad from University of Brasilia, Professor Eric Kerhervé and Associate Professor Nathalie Deltimple from University of Bordeaux.

Both students spent 18 months in France and were able to design and prototype CMOS circuits connected to the research topic.

1.2 GOALS OF THIS WORK

As part of the discussed cooperation, this work had the main goal to study, design and measure an RF power oscillator dedicated to communication standards. Further results include the study of the technical viability of direct modulation of the oscillator in order to obtain a system closer to the one depicted in Figure 1.3.

1.3 MAIN CONTRIBUTIONS

The main contributions of this work are listed and commented in the list below.

- The study of waveform engineering to address the problem of voltage stress in switched power amplifiers;
- The use of class EF2 circuits in RF, which will be presented in Chapter 2;
- The design and measurement of class EF2 power amplifier;
- The design and measurement of class EF2 power oscillator;
- Study of the direct modulation of a power amplifier and the presentation of theoretical limits;

1.4 ORGANIZATION OF THE DOCUMENT

In order to provide an overview on the research topics made in this work, related work on RF amplifiers, oscillators, some waveform engineering techniques and reconfigurable RF transmitters are presented in Chapter 2.

The design methodology for analog integrated circuit design and the measurement procedures are presented in Chapter 3. The used methodology for the design of the power amplifier and power oscillator are also shown. Specific comments are made about the measurement of each prototyped circuit.

Simulation and measurement results are presented in Chapter 4. The results include some theoretical analysis on direct modulation of oscillators, design and measurement of the designed power amplifier and power oscillator, a discussion on simulation issues and the proposed RF transmitter architecture.

The conclusions, future work and list of publications are presented on Chapter 5.

2 BIBLIOGRAPHICAL RESEARCH

This Chapter describes the theoretical background needed to evaluate this work. Among the different subjects covered in this text, special attention will be given to the following topics: (i) power amplifiers (with a special discussion about class E switched power amplifier), (ii) voltage stress in power amplifiers in modern CMOS technology, (iii) oscillators and power oscillators, (iv) common RF transmitter architectures and (v) issues on the used technology.

2.1 COMMUNICATIONS STANDARDS

High throughput mobile communication is already reality in many countries. The LTE (Long Term Evolution) has come up as a solution as a world wide standard for mobile applications. Managed by 3rd Generation Partnership Project (3GPP), this standard requires features that push the technological limits of IC design such as [7]:

- scalable channel bandwidth from 1.4 MHz up to 20 MHz;
- center frequencies from 700 MHz (in band 12) to 3500 MHz (in band 22);
- compatibility to the implemented systems;
- different modulation schemes, from QPSK to 64-QAM.

The standard also defines several criteria for ACPR (Adjacent Channel Power Ratio), output power levels and transmission quality, to name a few. All these specifications have a direct impact on the circuit performance and the document [7] concerns only the user equipment. Other parts of the network hardware are specified in similar documents.

Both Brazil and Europe share the specification of use of the band around 2.5 GHz. For this reason, all this work is made in this band. The viability of the solutions shown here do not depend on frequency and a redesign would be necessary to address other frequencies.

The items shown above present the the need of a very flexible hardware, that is able to be reconfigured depending on the situation of use. This work studies a reconfigurable RF transmitter based on an innovative architecture.

Futher information about LTE can be found in 3GPP website or in [8].

2.2 ARCHITECTURE OF RF TRANSMITTERS

This section presents an analysis on basic transmitter architectures: homodyne and heterodyne. A brief discussion is made about the advantages and limitations. The goal is to understand why these architectures are difficult to be made reconfigurable and flexible in order to address the multistandard requirements discussed earlier.

2.2.1 Homodyne

Homodyne transmitters are characterized by direct frequency conversion from baseband to the desired RF frequency. The block diagram is shown in Figure 2.1. In this Figure, the orthogonal components I and Q are considered to be already modulated either by analog or digital means. The mixers are responsible for frequency conversion. The carrier frequency is generated by a PLL that is omitted. Notice that the RF power contained in the carrier frequency generated by the PLL is often very low, only enough to create a voltage to drive the LO input of the mixers. It is also important to notice that, as components I and Q are orthogonal, the RF carrier must also be composed of two orthogonal components. The adder is responsible for building the modulated RF signal that must be power amplified by the PA. The matching network is responsible for presenting the correct impedance to the output of the PA and the duplexer makes the connection among the antenna and the transmit and receive paths.

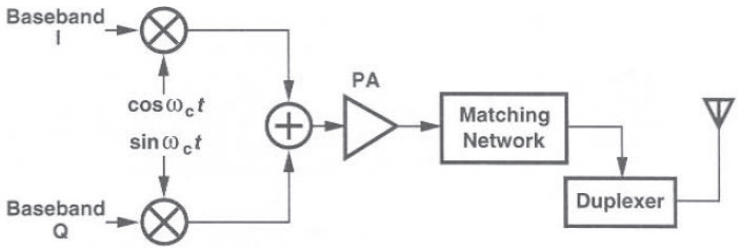


Figure 2.1: Direct conversion transmitter [9]

In real world implementations, all circuits are optimized to a given frequency band with linearity and frequency characteristics defined by the desired modulation scheme. Changing these parameters would demand alterations in the hardware which are often not possible. In Figure 2.1 filters for spurious attenuation are also omitted. These highly selective filters are also hard to tune.

Despite the difficulty in turning the transmitter in a multistandard system, this architecture suffers from serious drawbacks. One of them is the disturbance of the carrier generator by the PA. A fraction of the powerful modulated signal generated by the PA reaches the VCO through the substrate creating a “noisy” carrier due to injection pulling or locking. This effect is very common in modern technologies that use a highly doped, low impedance, substrate and which makes it difficult to be solved by shielding [10].

Another problem that may occur is the so called I/Q mismatch. Difficulties in generating carrier signals exactly 90° apart generate component signals that are not orthogonal in the carrier frequency causing intersymbol distortion, increasing EVM (Error Vector Magnitude). In the modulation constellation this can be observed by a moving or rotating the ideal constellation [11]. In some part because of these two

problems direct conversion architectures are less common than multiple conversion counterparts.

2.2.2 Heterodyne

In order to address these two serious problems, the heterodyne architecture (with multiple frequency conversions) have been proposed [12] and a typical block diagram is shown in Figure 2.2. Because of the different frequencies among the modulated RF signal generated by the PA and all the oscillators in the system, the problem of leakage is mitigated. The signal still leaks but it causes negligible (if any) effects. The generation of the modulated signal is made in an intermediate frequency where the phase imbalance is better controlled.

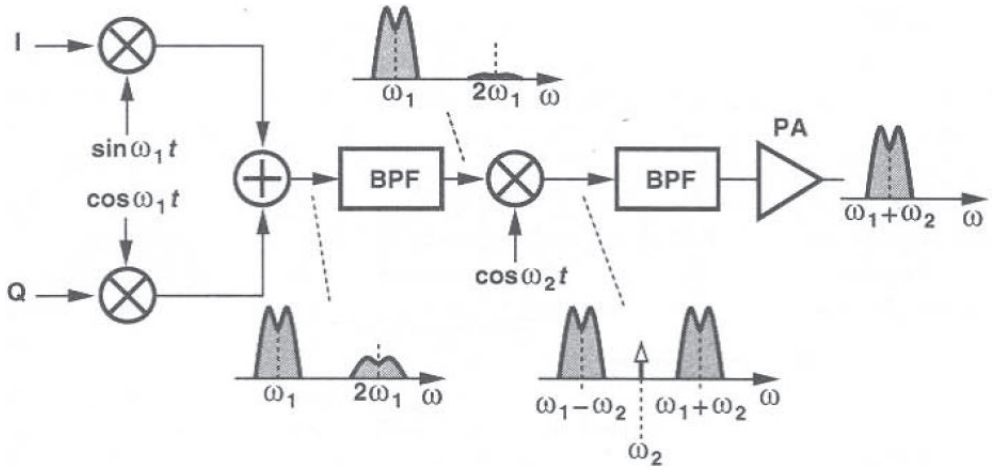


Figure 2.2: Two-step conversion transmitter [9]

The solution for the leakage and I/Q imbalance comes at the expense of a larger complexity and power consumption as more blocks are needed. The reconfigurability problem then is increased as more blocks needs to be reconfigurable.

The trend towards reconfigurability and integration are present in RF architectures as digital interfaces are pushed further and further towards the RF circuitry. Some examples of this trend are shown in [13]. Being configurable by software, the digital circuitry around the RF circuits could lead more flexibility. Rethinking the RF part, then, becomes necessary to replace the several separate circuits and reduce the need for filtering.

2.2.3 Towards a Simpler Architecture

The classical transmitter architectures present one characteristic in common: both deal with frequency translation using mixers. Being RF circuits, mixers tend to be tuned circuits. In addition, when the filtering provided by the mixer itself is not sufficient to fulfill the specifications, filters banks are included.

Even though work on reconfigurable RF circuits can be found, maintaining the efficiency and performance is very hard [14][15][16]. This fact leads to the use of specialized transceivers for each communication standard instead of one reconfigurable transceiver. The use of one reconfigurable transceiver could

simplify the PCB on which the final product is mounted, reducing design costs and increasing robustness.

The use of a circuit that can be directly modulated by a baseband signal and be directly connected to the antenna leads to a much simpler transmitter architecture, in which fewer RF circuits are used. The proposed architecture is presented in Figure 1.3 and repeated here for convenience.

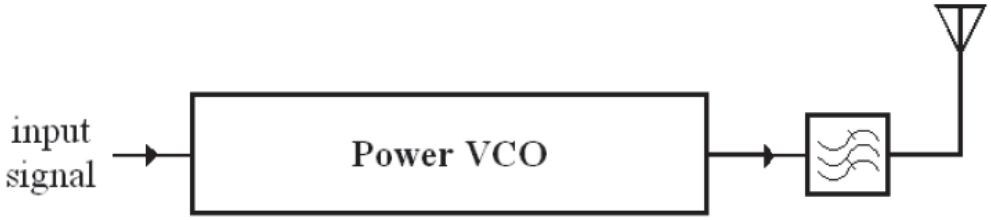


Figure 2.3: Transmitter based on Power Oscillator [4]

In this way, the problem of reconfigurability is separate in two simpler problems: (i) generate the correct input signal, which can be achieved by digital or analog base band processing and (ii) designing a power oscillator that can fullfil the specifications. Notice that the problem of designing many RF building blocks is now reduced to one circuit.

2.3 POWER AMPLIFIERS

Being the center topic of this work, a discussion on power amplifiers must be made. In the transmit chain, the function of the power amplifier is to deliver to the antenna a modulated signal with some quality parameters in sufficient power levels to be received with reasonable quality after the channel's attenuation and distortion. In this context, sufficient and reasonable quality are defined by the desired communication standard.

The specifications of the PA will be strongly dependent on the desired modulated signal, due to an intrinsic trade-off between linearity and efficiency that will be discussed in later sections of this Chapter.

In modern portable devices, the end user's satisfaction is very dependent on the battery lifetime. As the power amplifier is normally the most power hungry circuit of the transmit chain, a well designed power amplifier can have significant impact on the such experience. In order to maintain the usage time, an efficient power amplifier can lead to smaller, lighter and cheaper batteries affecting the whole product.

2.3.1 Key Parameters of Power Amplifiers

In order to be able to compare different power amplifiers, well defined figures of merit are needed. Important definitions are made with the help of Figure 2.4.

In Figure 2.4, a power amplifier is driven by a power source E_g that presents output impedance of Z_s. The load connected to its output is Z_L. The input and output impedances of the power amplifier are Z_{in} and Z_{out}, respectively. The input and output power are P_{in} and P_{out}, respectively. P_g is the power available from the source and P_L is the power delivered to the load. The DC input power is P_{DC} and P_{diss}

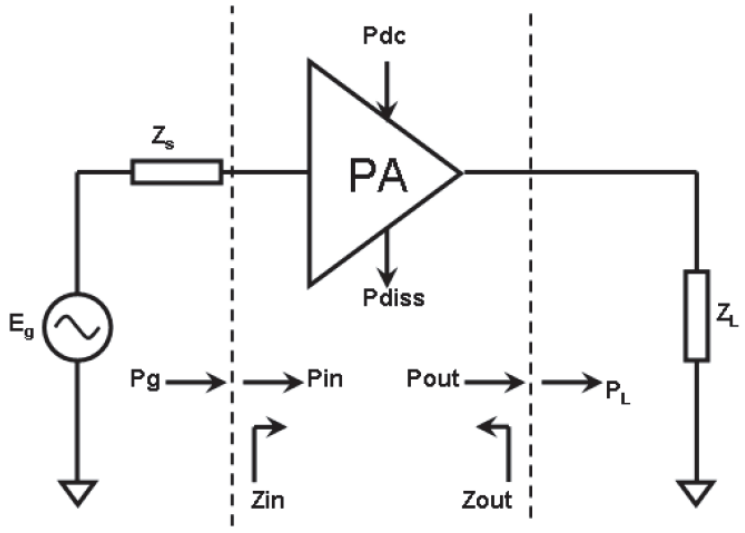


Figure 2.4: Important definitions of a power amplifier [17].

is the power dissipated by the amplifier.

Considering that the input and output impedances are matched, $P_g = P_{in}$ and $P_{out} = P_L$. This situation is common and desired, since no power reflection is desired. Considering the impedances are matched, the power gain is defined as:

$$G = \frac{P_{out}}{P_{in}} \tag{2.1}$$

It is also important to define efficiency for a power amplifier. In this context there are two widely used definitions [18]:

1. Drain efficiency (η): in this text the acronym DE will be used for this parameter. It quantifies the efficiency of the DC power into RF power. It is calculated as follows:

$$\eta = \frac{P_L}{P_{DC}} \tag{2.2}$$

2. Power Added Efficiency: in this text the acronym PAE will be used for this parameter. It also quantifies the efficiency of the DC power into RF power but takes into account the power needed to drive the amplifier. It is important to notice that the PAE will tend to DE when the power gain is large, because lower input power is needed to generate the same output power. It is calculated as follows:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \eta\left(1 - \frac{1}{G}\right) \tag{2.3}$$

As power amplifiers must often be able to deal with large signal swing, this type of circuit is frequently under operating conditions that lead to signal distortion, specially when operating close to the maximum output power. It is important to be able to understand the notion of gain compression. The AM/AM

characteristic depicts how output power, and consequently power gain, behaves as a function of input power. The typical AM/AM characteristic of a PA is shown in Figure 2.5. In this Figure, typical curve shapes are shown for output power, PAE and Drain Efficiency (η). Also depicted in Figure 2.5 is the so called "1 dB output power compression point"(OCP1) and this parameter is defined as a 1dB output power deviation from the ideal linear curve. Under high input power levels it is possible to observe that the output characteristics deviate from the ideal linear response. When the PA operates above OCP1, the amplifier is said to be compressed. A complete description and analysis of these distortions are not in the scope of this work and further information can be found in [19].

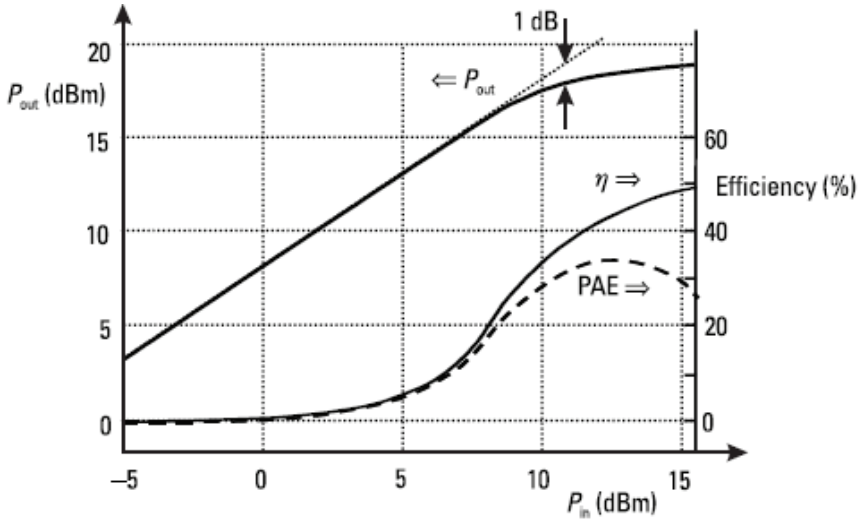


Figure 2.5: Fictional AM/AM characteristics[20].

It is in the compression region that the amplifier's efficiency reaches its maximum, because the output power is maximum. For that reason, from the efficiency point of view it is interesting to work at that region most of the time.

Along with the efficient (but non-linear) operation, distortion becomes an issue. Parameters such as ACPR (adjacent channel power ration) [18] quantifies the amount of harmonic content generated by the amplifier in amplitude domain. This parameter is specified for each communication standard and has the goal to protect the adjacent channel from interference. One way to estimate this parameter in simulation is to apply two tones to the input of the amplifier and study the output spectrum. Even order intermodulation will fall inside the communication band raising the power in the adjacent channel.

It is important to notice that no information is given about phase distortion. The existence of uncompensated phase distortion may cause symbol error in phase modulated signals such as PSK or QAM and increase EVM measurements. Typical AM/PM characteristics are shown in Figure 2.6.

This type of non-linearity is a direct result of current clipping and overdrive and often demands linearization. Linearization schemes will be treated later in the text.

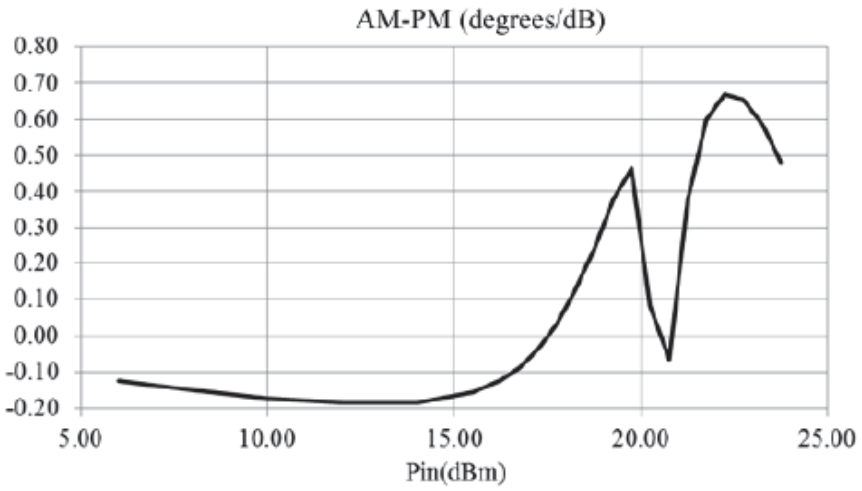


Figure 2.6: Typical AM/PM characteristics [21].

2.3.2 Combinantion of Stages

In order to obtain larger power gain, a power amplifier may be composed of more than one stage. In the case of having a power amplifier composed by 2 stages, the total gain, in dB, is given by:

$$G_T = G_1 + G_2 \tag{2.4}$$

In Equation 2.4, G_1 and G_2 represents the gain of first and second stage, respectively, while G_T is the total gain of the power amplifier.

The PAE of the composite amplifier is given by [22]:

$$PAE_T = \frac{\eta_2}{1 + \frac{\eta_2}{\eta_1 \cdot G_1 \cdot G_2}} \tag{2.5}$$

Equation 2.5 states that the overall efficiency is dominated by the efficiency of the 2nd stage if the gain of the power amplifier is large. Bearing this result in mind, it is feasible to use a driver to increase the power gain and still obtain an efficient power amplifier.

2.3.3 Classical trade-off in Power Amplifier Design

As shown in Figure 2.5, linear operation is frequently obtained at high backoff. In this situation, the output power is far from the maximum power and, thus, the efficiency is low. This fact exemplifies a strong trade off in power amplifier desing: linearity x efficiency.

Techniques have been proposed to increase the efficiency at high backoff at the expense of circuit complexity such as Doherty technique [23] but these issues are beyond the scope of this text.

In order to be able to control the trade off as a function of the desired specifications, it is possible to alter the biasing of the active device leading to different operating classes. Power amplifiers can be classified in

two broad categories:

- "Sinusoidal": in this category, the active device is used as a controlled current source. Examples are classes A, AB, B and C. The difference among these classes is the biasing conditions of the active device, which changes the conduction angle.
- Switched: in this category, the active device is used as a switch. Examples are classes D, E and F. The difference among these classes is the waveform the switch deals with.

A complete analysis on the design of each class is made in [19]. In this text a small description about the operating classes is made for comparison purposes.

2.3.4 Sinusoidal Classes

All "sinusoidal" amplifiers could be built using a common-source amplifier with an inductive load and an output matching network as shown in Figure 2.7. Changes in the class of operation come from a change in the bias voltage of source V_{in}.

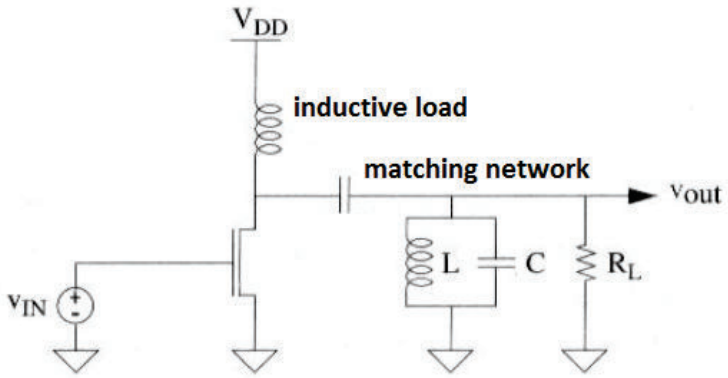


Figure 2.7: Circuit topology for sinusoidal PA [24].

2.3.4.1 Class A Power Amplifiers

Class A is defined when the DC bias voltage of the transistor is such that it is able to conduct current the whole time. An other way of stating this is saying the conduction angle is 360°, which means the transistor conducts current the whole cycle. Considering a first order transistor model for simplicity, in class A, the transistor must be always on. Which leads to:

$$V_{IN} \geq V_{th} \tag{2.6}$$

There are two ways of obtaining such a behavior: (i) maintaining the input voltage swing and increasing the DC biasing or (ii) maintaining the DC biasing and reducing the input voltage swing. The first approach increases the DC current, increasing the power consumption to make the amplifier achieve larger maximim

output power in class A. The second approach has the exact opposite behavior, reducing the output power to maintain the transistor biased in class A. It can also be shown that these changes in the signal do not alter the theoretical efficiency [19].

In this class, as the transistor is always carrying current, the transistor voltage-to-current characteristics are never chopped leading to higher linearity. This linear behavior is achieved at the expense of efficiency as much DC power is used to bias the transistor. The voltage and current waveforms are shown in Figure 2.8.

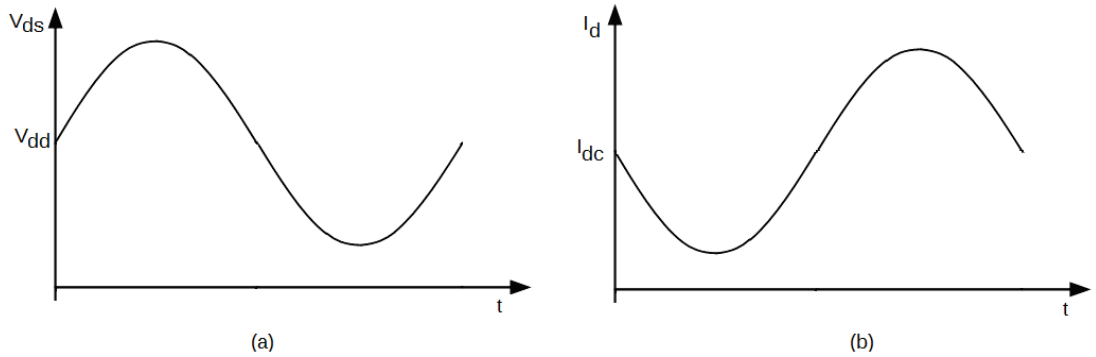


Figure 2.8: Class A waveforms: (a) voltage and (b) current.

Assuming all devices are lossless and that the transistor is an ideal transconductor ($v_{ds_{sat}} = 0$), the theoretical maximum efficiency can be shown to be 50% [25]. This value of efficiency leads to heating problems and low usage time in battery powered devices. This is obviously a very optimistic limit and its assumptions also lead to an important discussion on the voltage stress the transistor must be able to sustain. When operating at the maximum theoretical output power, the transistor must be able to sustain voltages up to $2V_{dd}$. This becomes a serious issue assuming that device scaling forces reductions in breakdown voltage [24].

As a conclusion, class A power amplifiers delivers linearity at the cost of low efficiency and relatively large device stress. For these reasons, class A amplifiers are rare in RF applications [24].

2.3.4.2 Class B Power Amplifiers

Still considering the first order transistor model, biasing the transistor exactly at the threshold voltage, leads to 180° conduction angle, meaning that the transistor would conduct current for exactly half a cycle. As in reality the device does not turn on abruptly, class B is an idealization but serves well for categorization purposes.

Reducing the conduction angle, reduces the DC power dissipation, potentially leading higher efficiency. As the current would be chopped in 50% of the duty cycle, the output power is non-sinusoidal and harmonics are generated, polluting side bands if proper care is not taken. On the other hand, the circuit is able to deliver proportional input-output power characteristics, addressing the problem of power amplification.

At maximum output power, it can also be shown that the theoretical maximum efficiency is 78,5% maintaining the voltage stress up to $2V_{dd}$. In class B, efficiency is traded for linearity, exemplifying this

common design decision. The ideal class B voltage and current waveforms are shown in Figure 2.9.

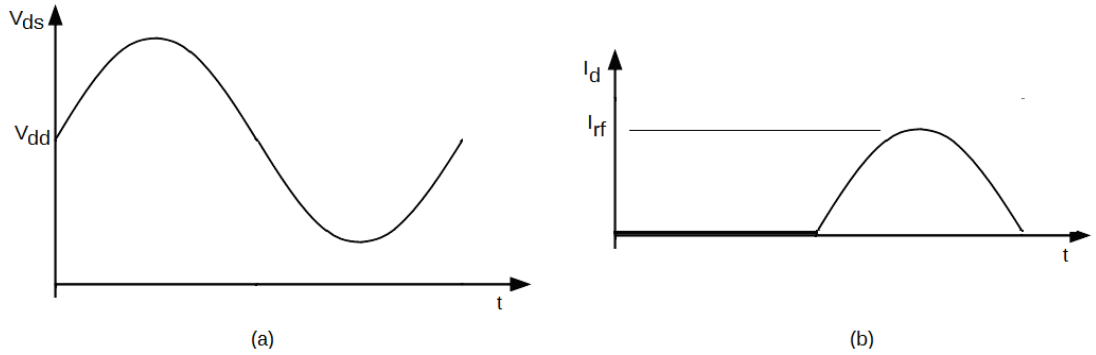


Figure 2.9: Class B waveforms: (a) voltage and (b) current.

It is important to comment class AB power amplifiers. This class is obtained when the conduction angle is kept any value between 180° and 360°. The efficiency increases as the operation leaves class A towards class B and voltage stress issues are kept constant when operating at maximum power.

2.3.4.3 Class C Power Amplifiers

Keeping the tendency of reducing the DC bias voltage of the transistor, reduces the conduction angle to values lower than 180°, leading the transistor to conduct less than half of the period. The drain current consists of a periodic train of pulses. The non-linearity is stronger than in class B as the current leaves the sinusoidal-like shape and tends to train of pulses. The harmonic content is also increased. The fictional class C voltage and current waveforms are shown in Figure 2.9.

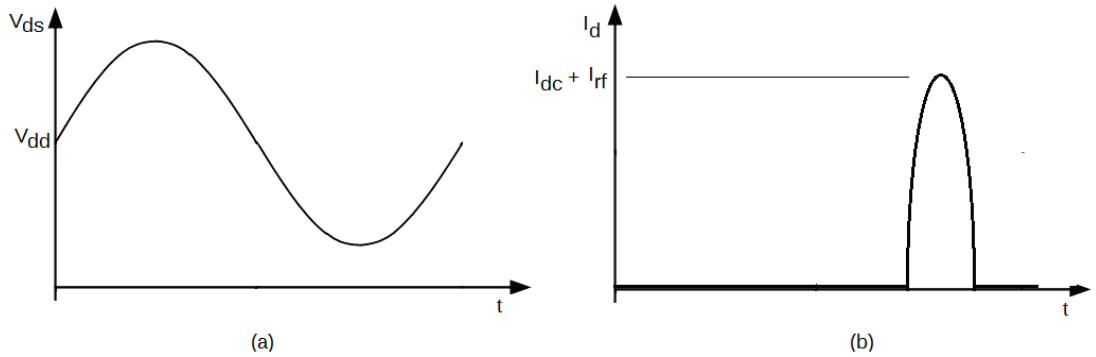


Figure 2.10: Class C waveforms: (a) voltage and (b) current.

The biasing conditions with a fictional input swing, a representation of the conduction angles is shown in Figure 2.11

Considering 2Φ the total conduction angle, Equation 2.7 [25] describes how the theoretical efficiency varies once the conduction angle is changed.

$$\eta_{max} = \frac{2\Phi - sin(2\Phi)}{4(sin\Phi - \Phi cos\phi)} \tag{2.7}$$

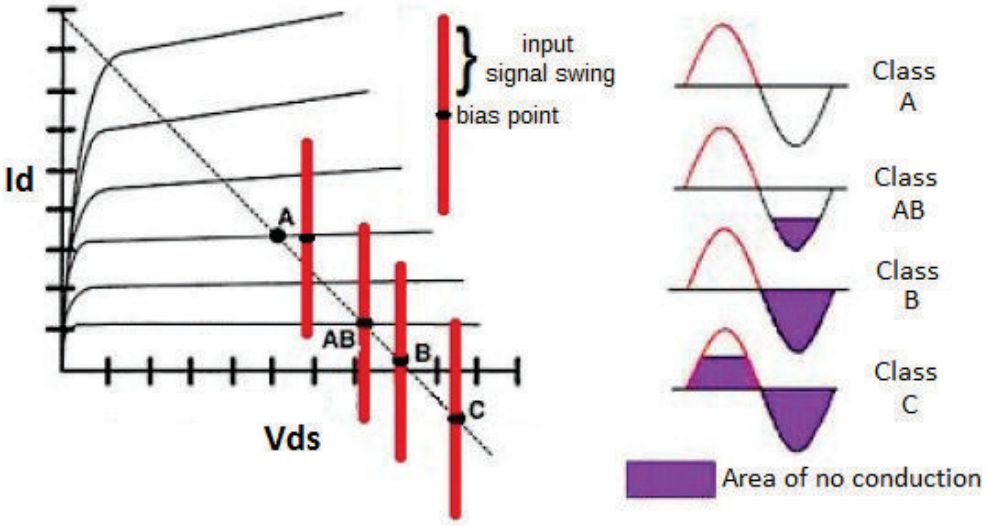


Figure 2.11: Representation of biasing scheme and conduction angle.

In fact, Equation 2.7 is general and can be used for any conduction angle, from class A to deep class C. The evolution of efficiency and normalized output power with the operation class is shown in Figure 2.12.

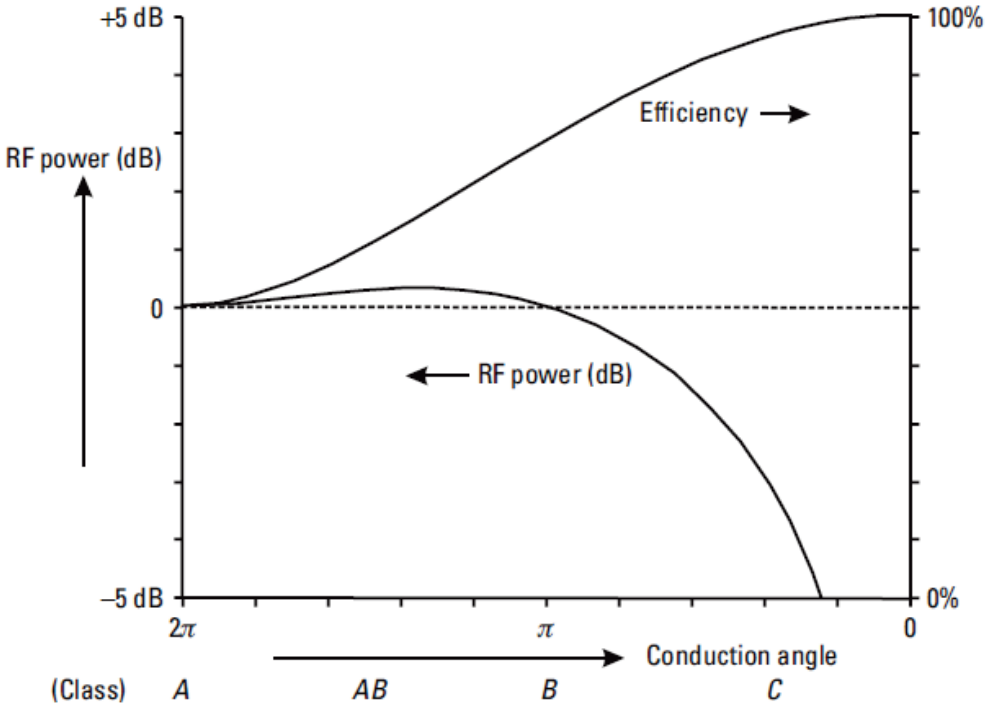


Figure 2.12: Efficiency and output power as a function of the operating class [19]

Some interesenting aspects can be observed in Figure 2.12. First of all, the manner the efficiency depends on the conduction angle is shown. When operating near class A, a reduction in the conduction angle leads to marginal increase in efficiency. The same asymptotic behavior is observed in deep class C.

Regarding the power handling capability (normalized with respect to class A operation) also displays important characteristics. In ideal class B, the circuit is capable of dealing with as much power as its class

A counterpart. The difference would be the efficiency and harmonic content generation. As the conduction angle is reduced, the power handling capability is also strongly reduced leading to the paradoxical 100% efficiency but no output power. This effect can be explained by the fact that the current pulses become narrower as the conduction angle is reduced, ultimately not allowing any current to flow.

The increase in power handling capability observed in class AB can be explained by an increase in the current flowing in the fundamental frequency. As a consequence of the non-linearity, harmonic content is generated. It is shown in Figure 2.13.

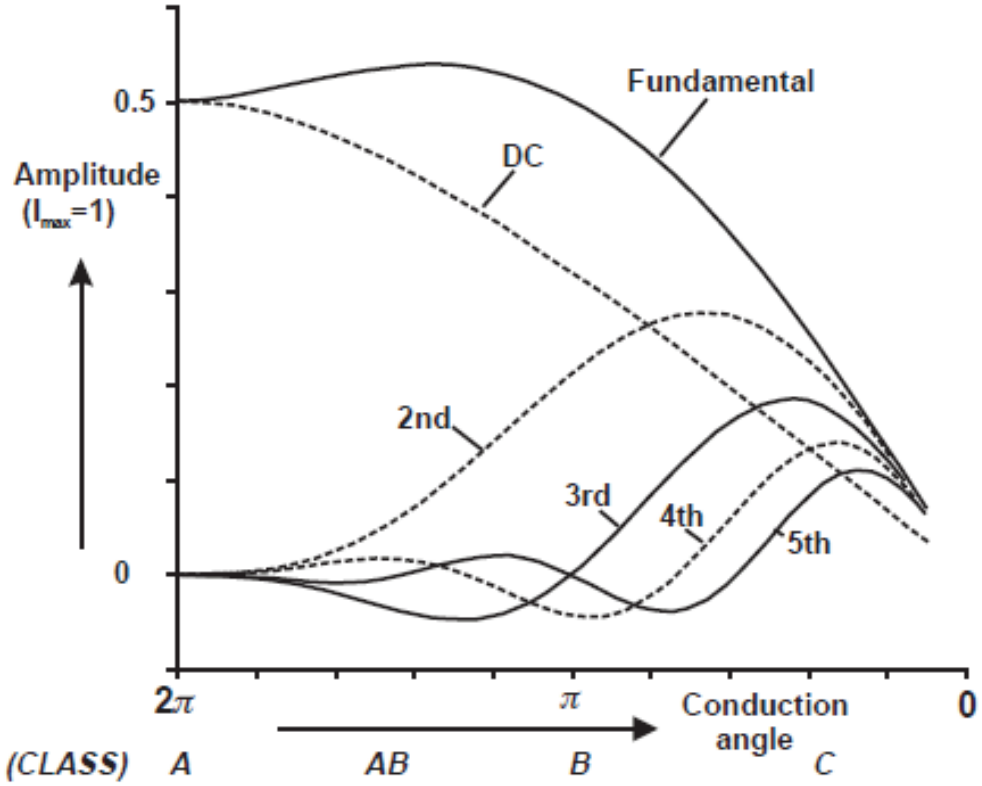


Figure 2.13: Harmonic generation as a function of the operating class [25]

A reduction in the DC component is explained by the reduction in the quiescent current flowing through the transistor. Power in the 2nd harmonic grows rapidly affecting the power leakage to adjacent channels. It can be observed that as the conduction angle is reduced, stronger non-linearity is obtained as expected. The combination of Figures 2.12 and 2.13 clearly show how the linearity versus efficiency trade off is present in power amplifier design.

As the transistor is used as a current source in sinusoidal classes, in order to obtain maximum power, full voltage swing is needed. In this sense, all sinusoidal classes present similar voltage stress across the transistor, ideally $2V_{dd}$.

2.3.5 Switched Classes

In this section, switched classes are discussed. Treating the transistor like a switch, instead of a current source, can, ideally, lead to 100% efficiency. The discussion starts with class D and follows on to class E.

2.3.5.1 Class D

A class D amplifier is shown in Figure 2.14. Observing the biasing of the transistor, it is normally off as $V_{gs} = 0$. Considering $V_{th} = 0$ for simplicity, each transistor of Figure 2.14 is biased in class B. They share one side of a transformer that serves as DC feed.

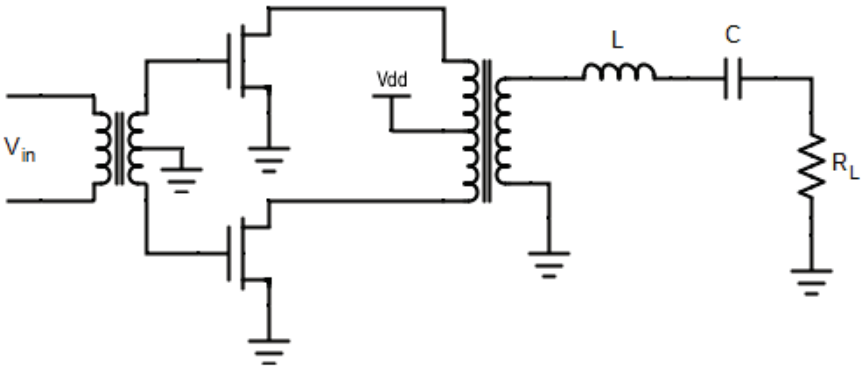


Figure 2.14: Class D amplifier

Considering that inductor L and capacitor C form a high quality factor series LC tank tuned to the fundamental, the only frequency allowed to flow through R_L is the fundamental. The basic difference between a class B and a class D amplifier is how the transistors are driven. In class D power amplifier, the transistor are driven hard enough to make them behave as switches, either off or in deep triode region, with a low R_{on}.

The voltage on the drains of the transitors vary between 0, due to switching, and $2V_{dd}$, due to reaction from the transformer and, if the switch is considered ideal, theoretical efficiency of 100% is achieved [24]. As the transistor is operated as a switch, it is ideally, impossible to control the output power with respect to the input power, i.e., the amplifier operates in compression. A reduction in the input power, may lead the transistor not to operate as a switch. This would lead to a not correct class D operation, thus, reducing the overall efficiency.

As the efficiency depends on non overlapping voltage and current waveforms, very sharp switching is necessary of the correct operation in class D and, consequently, high efficiency. Often the transistor sizes are made very big in order to reduce R_{on}, reducing the switching speed due to parasitic capacitance. This characteristic limits the use of class D amplifiers in many applications but works using this class have been reported [26].

2.3.5.2 Class E

Class E circuits take advantage of reactive components in order to obtain high efficiency. The ideal class E circuit is shown in Figure 2.15. The transistor is used as a switch and, hence, in large signal operation. The passive components used are L_{choke}, C_{sh}, L_0 and C_0. The resistor R_{load} represents the load seen at the terminal of C_0.

The idea behind switching-mode PA, such as class E, is designing the time domain voltage and current

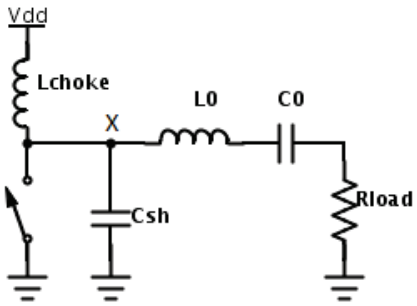


Figure 2.15: Ideal class E circuit

waveforms in a way they never overlap. Notice here that the mentioned voltage is at point X (across the switch) and the current through the switch. If there is no overlap between these two waveforms, the transient power dissipation on the switch is always zero, leading to high efficiency. The ideal time-domain waveforms are shown in Figure 2.16 and the ideal output power is given by Equation 2.8, where k is a constant dependent on the class and V_{dd} is the supply voltage.

$$P_{out} = k \cdot \frac{{V_{dd}}^2}{R_{load}} \tag{2.8}$$

Mathematically, class E operation is obtained if Equations 2.9 and 2.10 are simultaneously solved.

$$v_x(t_1) = 0 \tag{2.9}$$

$$\frac{\delta v_x(t_1)}{\delta t} = 0 \tag{2.10}$$

It can be shown that the output power is related to the discontinuity in the current waveform as the switch opens [27]. The voltage waveform is designed to meet zero voltage switching (ZVS) and zero voltage slope switching (ZdVS) conditions. ZVS establishes that the switch closes when voltage waveform achieves zero voltage while ZdVS estates that the derivative of the voltage should also be zero when the switch closes. The ZVS condition is essential for the non overlapping waveforms while ZdVS is used to minimize overlap in case of parameters or frequency variations.

In high frequencies, at the moment of the switch commutation, some overlap between voltage and current occur and, as the curret is often high at this moment, losses are not negligible. One way to address this issue is to use the called class E_m: This class fulfils conditions presented in Equations 2.9 and 2.10 also for the current across the switch. In its name, “m” stands for microwave. This higher efficiency is obtained at the cost of complexity as two power amplifiers are put to work in parallel. More discussion about this class is made in [28].

As the definition of class E circuits is made by time domain equations, the design methodology is basically made using time domain approaches. It is important to mention that Figure 2.16 is obtained for a normalized voltage and load class E circuit, i.e., $V_{dd} = 1$ and $R_L = 1$.

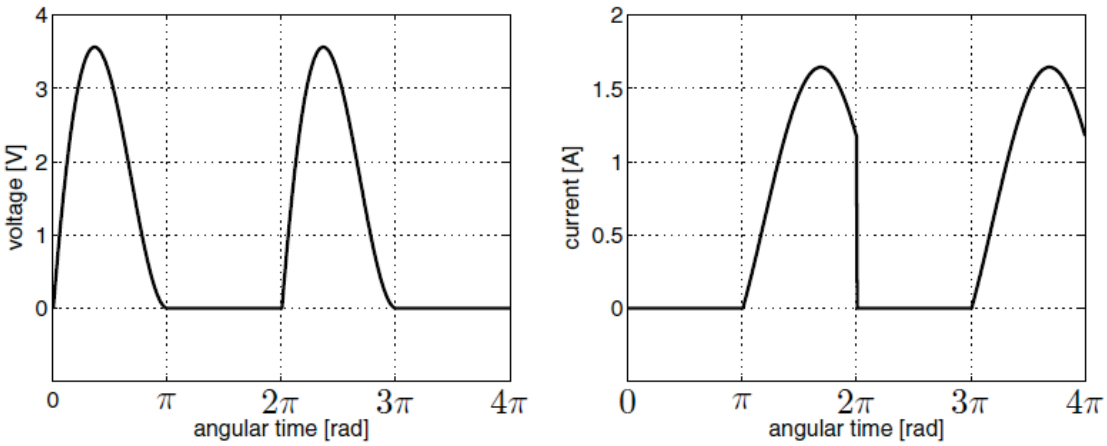


Figure 2.16: Ideal class E waveforms: (a)voltage and (b)current [27]

Despite the apparent simplicity of the schematic shown in Figure 2.15, the use of class E circuits is attractive in RF frequency due to the existence of capacitor C_{sh}. This capacitance is necessary for the correct operation in class E and can be implemented by the parasitic capacitance of the transistor. In this sense, the parasitic capacitance becomes necessary instead of a burden as it was shown to be in class D.

Assuming an ideal switch, the simultaneous solution of Equations 2.9 and 2.10 is obtained by the correct design of the passive network. The LC tank formed by C_0 and L_0 play two roles in the design. The capacitor C_0 and part of the inductor L_0 are dimensioned to be a filter tuned to the switching frequency. Supposing this filter has a high quality factor, a sinusoidal current flows through the load resistor, despite the non-linear behavior. The rest of inductance present in L_0, called excess inductance in [29], is used, along with C_{sh} to shape the voltage and current waveforms. This assumption is valid if L_{choke} is considered a real RF choke. In this way, it does not participate in the waveform engineering [27]. Ideal design equations are derived in [29].

Another issue is to design the switch. Assuming the transistor is being driven by sufficent power to set it to triode when it is ON, R_{on} can be estimated as shown in Equation 2.11:

$$R_{on} = \frac{1}{\mu_n C_{ox} W/L(V_{gs} - V_{th} - V_{ds}/2)} \approx \frac{1}{W} \tag{2.11}$$

It is clear that using large device width reduces the parasitic resistance and, therefore, it should be maximized to increase efficiency. Nevertheless, once R_{on} becomes smaller than the resistive losses in the passives, further increase in W does not affect the efficiency. On the other hand, the size of the device is limited by the parasitic capacitance needed to implement the passive network around the transistor. If the device width is increased beyond this point, correct class E cannot be obtained.

Concerning robustness of the solution, the presence of high voltages and high currents create the so called *hot carries*. They are very energetic carriers that can be injected in the oxide causing a shift in the transistor parameters and, in the long term, cause breakdown of the oxide. This problem is alleviated in class E amplifiers as voltage and current are non-overlapping [27].

Many works present the ideal waveforms expected for this kind of circuit, for instance [30]. This kind of circuit was proposed in [29] back in 1975. In [29], the time domain waveforms are presented as well as a design methodology based on closed form equations with idealized assumptions. In the ideal class E, a large impedance inductance is used as a choke, not allowing the AC current to vary along the time since this current is supplied by a large impedance in a similar way as DC current sources work. When the choke impedance is made high enough, its value does not affect the sizing of the other passive devices. A very extensive review about the class E power amplifier has been made in [27], including ideal equations, non-idealities and design guide lines. Special attention should be given to the methods of solving the class E equations in the presence of non-idealities as it leads to a optimized circuit that does not entirely fulfill class E definition in order to achieve highest efficiency.

Other works aimed at better understanding of the class E circuits and the literature on the subject is large. One work that summarizes the history of class E circuits is [27]. The authors also analyze the effect of a finite inductance instead of a choke, presenting the advantages and drawbacks. It is shown that the power capability of the amplifier is increased if a finite inductance is used, at the expense of a time varying AC current drained from the power supply. As the supply is often not capable of delivering high AC currents, large decoupling capacitors are needed to provide such current. One other drawback is the more complex design since the equations presented by Sokal [29] no longer apply and the value of the inductance affects all other device values.

A study on different passive networks able to deliver class E waveforms is made in [31]. This work uses the finite DC-feed inductance to present a class E power amplifier that presents no series resonating tank (L_0 and C_0 in Figure 2.15). As a consequence, upper harmonics are higher and narrow band operation is achieved. Other passive networks, such as the "parallel network circuit", capable of wideband operation, are studied in [31].

Several issues arise when implementing a class E circuit in modern CMOS technologies. In IC design, large inductances are hard to implement on chip and tend to be lossy. Thus, the implementation of on chip L_{choke} is not feasible. As the DC-feed inductance is comparable with L_0, it also has effect on the shape of the waveforms. Also the quality factor of L_0 leads to non-sinusoidal currents flowing through the resistor.

Class E PA also suffers from a well known drawback: the voltage stress across the switch is high, 3.56 times the supply voltage in the ideal case [29], depicted in Figure 2.16. As the output power is a strong function of the supply voltage, it is desirable to be able to work with higher supply voltages since reducing the load (R_{load} in Figure 2.15), leads to ohmic losses in the transformation network. On the other hand, modern CMOS technologies present lower breakdown voltage after each generation. These two facts pose a serious problem in designing high power CMOS class E PA.

One possibility is to use cascoded transistors in order to split the voltage stress among many devices. This approach is commonly used and can be found in [32], [33] and [34]. Although this approach adds the R_{ON} of another device, it allows an increase in the supply voltage. Roughly, if *n* transistors are stacked, the supply voltage can be increased by *n* and the load resistor made n^2 times smaller for the same output power. In this scenario, if the output power is kept constant, the current flowing through the switch is reduced by *n*, reducing the losses in the passives and in the switch.

Also using cascode switches, the works [35] and [36] deal with the parasitic capacitance added between the transistors. It is shown to be an important source of efficiency loss. Tuning this capacitance out with an inductor [32] [34] demands large area and is a narrow band approach. Instead of using inductors, a capacitor is used to implement a negative capacitance that subtracts the parasitics leading to higher efficiencies. Increases of around 2% to 3% were observed in the present work.

2.4 VOLTAGE STRESS IN POWER AMPLIFIERS

Class E circuits find great use in RF design due to its characteristics to use the parasitic capacitance in order to obtain high efficiency. Unfortunately, it comes at the expense of high voltage stress.

Instead of adding extra transistors to deal with the voltage stress intrinsic to class E, waveform engineering can be used to create an amplifier with certain interesting characteristics, such as lower voltage stress or greater power capability, for example.

Examples of the results given by this technique is shown in [37] and [38]. In these works, classes EF2 and E/F3 are discussed. These classes meet the ZVS and ZdVS but the voltage and current waveforms are improved.

The name of the class defines the implementation. In the case of EF2, ZVS and ZdVS conditions are inherited from class E and a short circuit to the second harmonic of the voltage is used. Presenting opens (high impedance) and shorts (low impedance) is typical in class F power amplifiers. In case E/F3, an open circuit is presented to the third harmonic of the voltage waveform. The waveforms for optimum operation for class E, class EF2 and E/F3 are shown in Figure 2.17. It is important to notice the change in the duty cycle D for each class of operation.

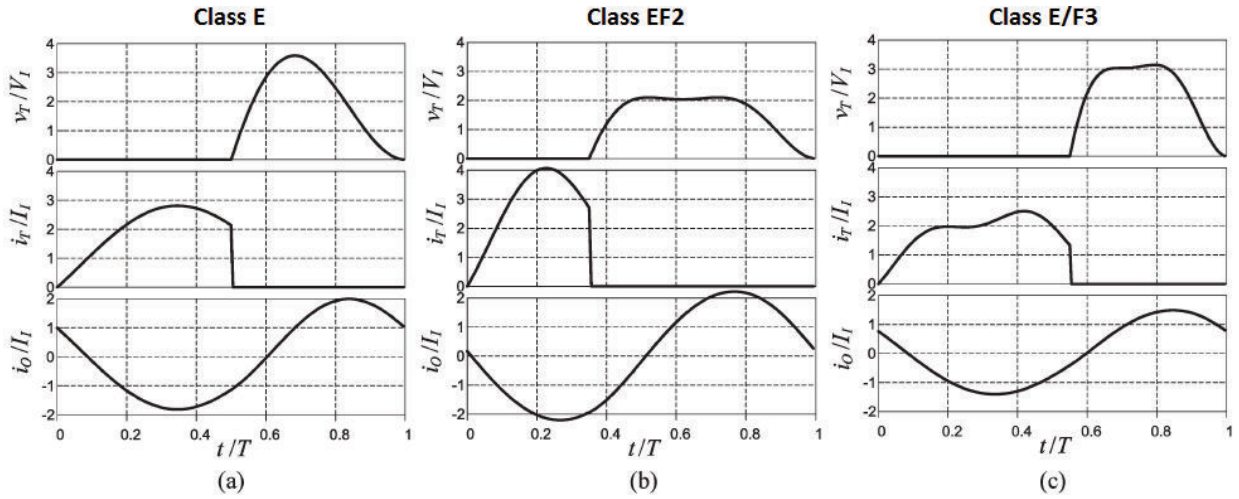


Figure 2.17: Waveforms for optimum operation. (a) Class E at D = 0.5. (b) Class EF2 at D = 0.35. (c) Class E/F3 at D = 0.55.[37]

In the first line of curves of Figure 2.17, the voltage across the switches are presented. The second line of curves present the transient currents and the last line of curves present the current on the load. Notice

the lowest voltage stress for class EF2 and, on the other hand, the current is the highest. Aiming at low breakdown voltage transistors, class EF2 is the most suitable solution because of the lower voltage stress demanded by this class. Figure 3.4 presents the ideal schematic of a class EF2 power circuit. In this circuit, L2 and C2 implement a series resonating tank that presents a short circuit across the switch.

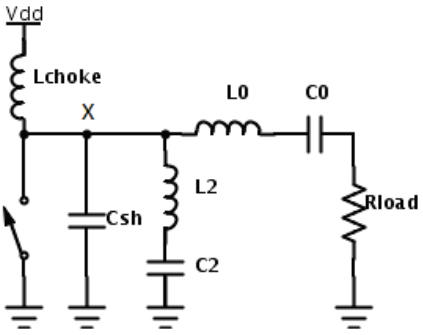


Figure 2.18: Ideal class EF2 circuit.

It is clear that the performance of the circuit for each class is a function of the duty cycle used. In the case of class EF2, the optimum duty cycle is 35%. Under this condition, not only the voltage stress across the switch is lower than class E with 50% duty cycle (which is chose to the optimum) but also the power handling capability is 43% higher. The power handling capabilities (C_{pmr}) for different duty cycles are shown in Figure 2.19. This dimensionless parameter is related to coefficient k in Equation 2.8.

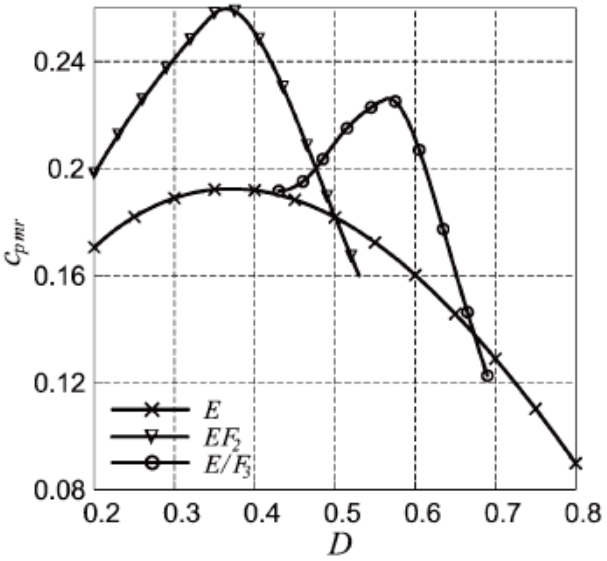


Figure 2.19: Output power capability versus duty cycle [37]

It is also possible to control the voltage stress on the switch by altering the duty cycle of the switching. Ideal voltages and currents for classes E, EF2 and E/F3 for different duty cycles are shown in Figure 2.20. The first line of curves in Figure 2.20 depicts the normalized voltages across the switch while the second line depicts the normalized current for several duty cycles. All axis are normalized with either voltage, current or period. The reduction in voltage stress come at the expense of reduction in power handling capabilities. Class EF2 presents a good alternative for higher power handling capability and

reduced voltage stress.

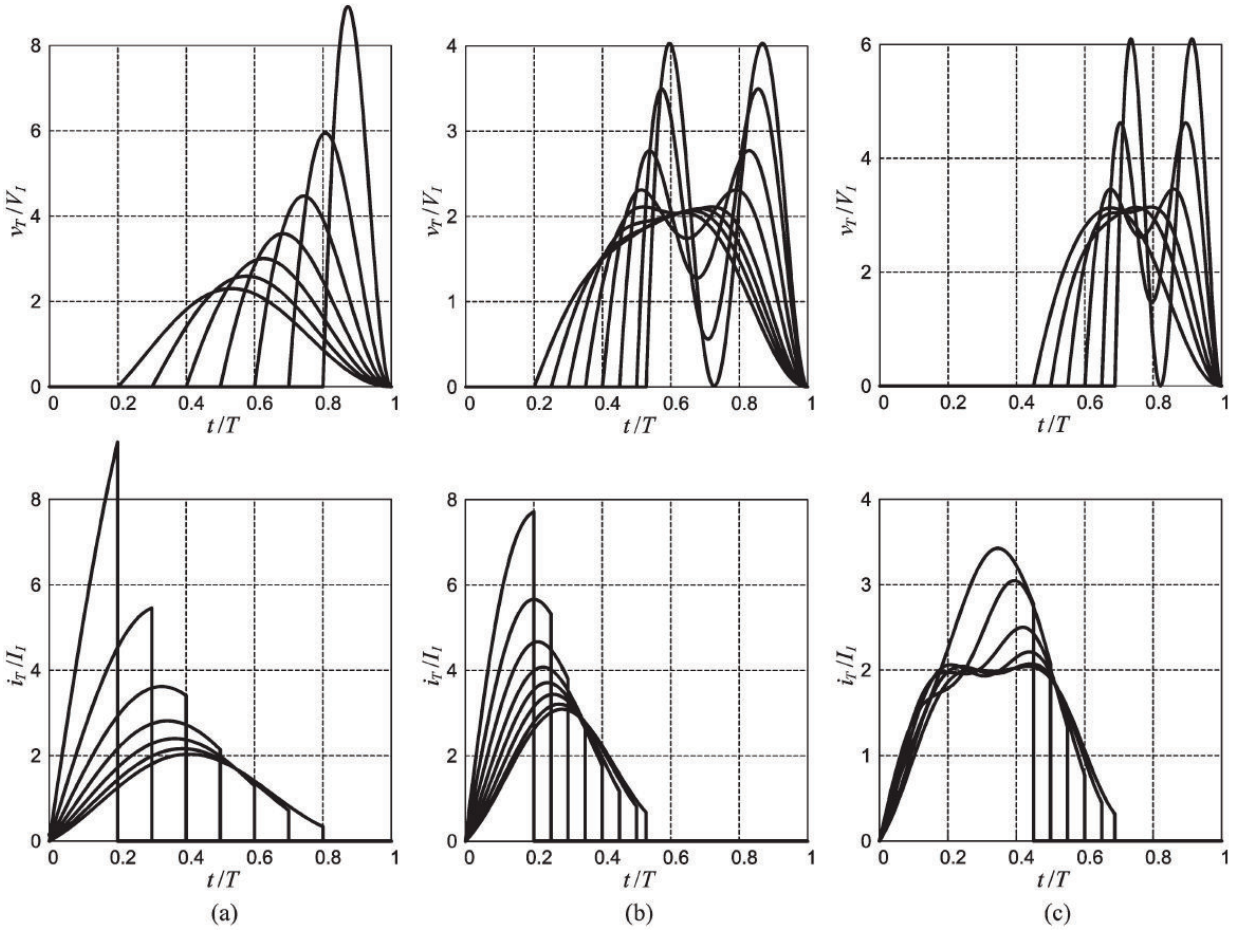


Figure 2.20: Normalized transistor voltage and current waveforms of (a) class E, (b) class EF2 and (c) class E/F3. [37]

Another interesting characteristic of the class EF2 circuit is in the output spectrum: the second harmonic of the generated RF signal have less power than the class E counterpart due to the short circuit presented to such harmonic. Figure 2.21 presents the output power spectrum for ideal class E and EF2 power amplifiers normalized with respect to the first harmonic. It can be seen that the second harmonic for class EF2 is around 20 dB lower than in class E. Although the third and fourth harmonics are higher in the ideal circuits, in practical realizations the circuit parasitics attenuate these upper harmonics leading to a more sinusoidal output power.

The use of this altered output spectrum is dependent of the creativity of the designer upon each concrete situation. As an example in communication applications, the weaker 2nd harmonic would alleviate the specifications on the filter between the PA and the antenna.

The discussion made so far, associated with the use of modern CMOS devices, worsens the classical trade off between efficiency and linearity, adding an other variable to it: robustness. Safe operating regions are provided by every foundry but some developed aging models that allow the designer to estimate the life span of the circuit under high stress operation. Supposing the circuit is correctly simulated and validated, the voltage stress above the safe region may be traded for high efficiency of linearity, still maintaining a

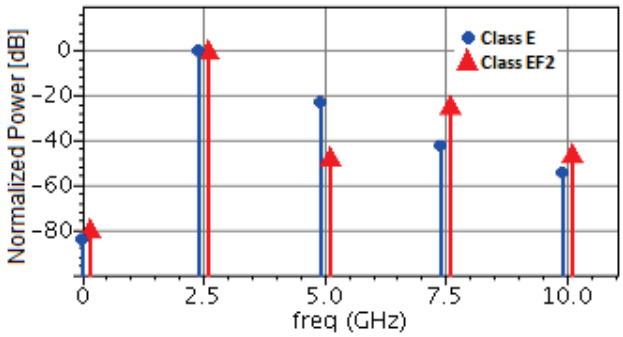


Figure 2.21: Normalized output spectrum for class E and class EF2 ideal power amplifier.

long life spam for the circuit.

The design of every integrated circuit begins with the choice of the technology that will be used. Issues such as maximum tolerable voltage, number of metal layers and high voltage options must be discussed. In case a given technology is not capable to deal with the desired power levels, it must not be chosen, despite the advantages it may bring such as ease of integration, the case of modern CMOS.

As already discussed, the efficiency is maximum when the PA operates compressed, near the maximum power it is able to deliver. Keeping the efficiency problem in mind, it is interesting to make the output power as high as possible for a given PA. Observing the situation discussed in the previous paragraph, it is not rare to operate close to the limits of the technology in order to obtain lower cost and high efficiency. Therefore, very special care must be taken with the power devices since their lifetime may be reduced if high stress is applied on them. As entire systems converge to SoCs, the failure of one device may lead to the expensive replacement of the whole chip.

From the discussion made above it is possible to observe a trade off involving three main parameters of every product: robustness, efficiency and cost.Efficiency and cost are related to the efficiency of the PA and the choice of the battery. Robustness is related to the obtained efficiency and voltage stress applied on the power devices. A good compromise solution must be taken in order to make an efficient, as cheap as possible and able to work for an adequate time.

From a performance point of view, CMOS is not the best technology to be used in RF circuits. Substrates from III-V family such as GaAS provide larger carrier mobility and, hence, higher efficiency. Nevertheless, high level of integration is observed nowadays and circuits are becoming more and more complex. Due to CMOS scaling, millions and even billion devices are in the roadmap [39]. It is economically interesting to make complete systems on chip as large volumes are used to reduce the price per unit and simpler PCBs are needed. The only technology capable of such integration level is the modern CMOS and this trend validates the research on how to implement circuits efficiently in this technology.

As a consequence of CMOS scaling, the nominal supply voltages are gradually being reduced, increasing the issues on how to generate usable RF power levels (evidenced in Equation 2.8) with reasonable robustness. This statement holds true for every class of PA since the output power is related to the voltage swing on the power device and the current that flows through it.

In the context of switched PA, it is possible to increase the tolerable voltage stress by using cascode

switches. The biasing conditions are made in a way to split the stress accordingly to each device. As a rule of thumb [32] in order to obtain high efficiency, the common source device should be made as fast as possible while the common gate device is used to withstand large part of the voltage stress. For this reason, it is very common to find thin oxide transistors in the common source device and common gate transistor with thick oxide in the literature [35] [40].

The work presented by Mazzanti [32] presents the voltage stress in RF power amplifiers in 130 nm STMicroelectronics technology. One important conclusion is that as long as the transient voltage stress is kept below two times the nominal supply voltage, the lifetime of the device is not seriously affected. This presents an important design guideline for PA designs.

2.5 POWER OSCILLATORS

As RF transmitters tend to get more complex to address the different communication standards, certain blocks function are merged in order to reduce power consumption and wafer surface. In [41], a VCO is merged with a prescaler. More aggressive merging can be observed in [5] where the LNA and the mixer are desgined as one circuit and [42] where a merged mixer and the VCO are presented. In [43] the whole receiver front end is designed in a very compact and elegant circuit.

Following this approach in the transmit path, one might imagine merging the VCO and the power amplifier, giving rise to a new class of circuit called here a “power oscillator”. Generating a powerful oscillating signal that can be directly modulated could raise possibilities for rethinking the whole transmit path [4].

This circuit can be made out of an ordinary VCO whose output signal is amplified in order to be delivered to the antenna. As in the approach previously mentioned, the oscillator and the power amplifier are still clearly separated, another way to accomplish the desired function is to try to really merge the two circuits. It is known that every oscillator is based on a amplifier with some kind of feedback. Therefore, to accomplish a power oscillator, a power amplifier can have its output fedback to the input in order to sustain self oscillation.

The oscillation criteria, called Barkhausen Criteria [44], is a direct application of control theory of closed loop systems. This criteria states that, in order for a circuit to oscillate, the closed loop gain must be greater than the unity and the phase shift must be $2k\pi$, if the feedback is considered positive.

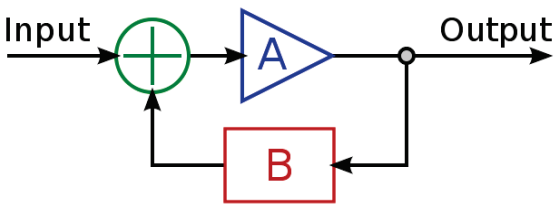


Figure 2.22: Block diagram of an arbitrary control system.

In the system of Figure 2.22, "A" is made with a power amplifier and the feedback network is implemented with a mix of an attenuator, in order to comply with the input power capabilities of the technology, and passive components, that assure the phase shift.

It is important to notice that despite the common practice in PA design, the input impedance of the power amplifier is not made 50 Ω. In order to be able to extract most power out of the oscillator, the feedback signal must carry low power, and, hence, it must be a voltage signal, with power as low as possible. Indeed an ideal voltage signal has zero power (it carries no current because the impedance is infinite) but the feedback signal must be able to drive a transistor that is often made large and presents large parasitic capacitance. This is a clear trade off between the achievable output power and the input impedance of the PA that can be obtained in the technology.

A block diagram of the described power oscillator is depicted in Figure 2.23. In order to be able to modulate the output power, control signals are added. Ctrl_1, responsible for AM modulation, is injected directly in the direct path of the oscillating loop, often in the supply voltage and Ctrl_2, responsible for phase control, is connected in the feedback loop. As it is known, every modulated signal s(t) can be written generically as:

$$s(t) = A(t) \cdot cos(\omega t + \phi(t)) \tag{2.12}$$

where A(t) is the amplitude component and $\phi(t)$ is the phase component. A transmitter based on this oscillator is capable of generating complex modulation schemes such as QAM. It is only a matter of generating the correct control signals.

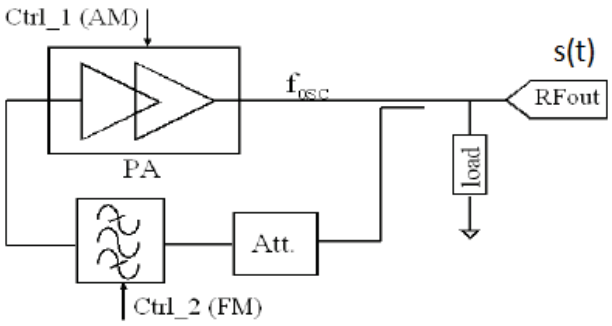


Figure 2.23: Power oscillator block diagram

The first publication on the subject, to the knowledge of the author, dates from 1981 [45]. In this work, a class E power amplifier is connected as depicted in Figure 2.23 with the use of a diode to deliver a square-like waveform to switch the transistors. Although the application is very different, using a frequency of 2 MHz, the concept is very similar. The circuit was able to deliver up to 3 W with 95% DC-RF efficiency. The high efficiency is mainly due to the low frequency switching which provides very low voltage and current overlap. It is important to notice that no modulation was applied to this circuit.

A design procedure was proposed in [46]. The procedure is based of considering the oscillator a forced circuit and sizing the components in order to fit the time domain waveforms. The designed circuit delivers 2.8 W with 89.7% efficiency around 1.98 MHz. Another design procedure for power oscillator design was

published in 2005 [37]. The designed circuit is topologically the same but operates around 800 kHz with smaller efficiency, around 82%. A third design approach was proposed in [47]. This work uses custom simulation infrastructure to design power oscillator. Their class E oscillator presents up to 75 W with 67% efficiency around 410 MHz.

Power oscillators operating around RF frequencies have also been published. In [48], an oscillator capable of 65 W with 65% efficiency around 915 MHz with double feedback loop is demonstrated. A power oscillator around 900 MHz with output power of 8.5 dBm and supply voltage of 1.2 V is presented in [49]. Inside ISM 2.4 GHz, an integrated power oscillator with 27 dBm and 42.5% efficiency is presented in [50].

In 2006, the team of Niknejad demonstrated an RF transmitter based on a power oscillator using injection locking for wireless sensor networks (WSN) applications [51]. The complete transmitter presents an overall efficiency up to 32% around 1.9 GHz with 0 dBm output consuming only 1.6 mW. Other approaches for modulating power oscillators have also been reported. For instance, in [52] a PLL is used to directly modulate a power oscillator using GMSK.

2.6 POWER AMPLIFIER LINEARIZATION TECHNIQUES

Knowing that usage time is essential in successful modern battery powered portable devices, the power amplifier must be used at maximum efficiency. It was shown in previous sections that efficiency comes at the expense of linearity and, for that reason, techniques to linearize efficient power amplifier have been developed. Non-linearities are often not tolerable as it increases EVM and pollutes adjacent channels.

In this Section, some of these techniques will be discussed as some of the have been used in this work.

2.6.1 Open Loop Strategies

One possible manner to linearize a system is to create a second system that is able to compensate it. Notice that this technique can be used for any system but is applied here for power amplifier. This technique is called “predistortion”. The first step to use this technique is to well characterize the non-linear power amplifier. Once the distortions, amplitude and phase, are well understood, a predistortion stage is designed in way to have the opposite non-linear behavior as shown in Figure 2.24.

The behavior of the combination of both stages is a linear power amplifier as it is desired. Although the idea seems simple, this approach suffers from a serious drawback: as it is open loop, any shift in the power amplifier is no longer compensated. Knowing the behavior of the power amplifier may shift due to aging effects, heating and memory effects, this technique finds use in base stations [53]. It is also possible to make predistortion adaptive based on feedback loops or look-up tables [54] [55].

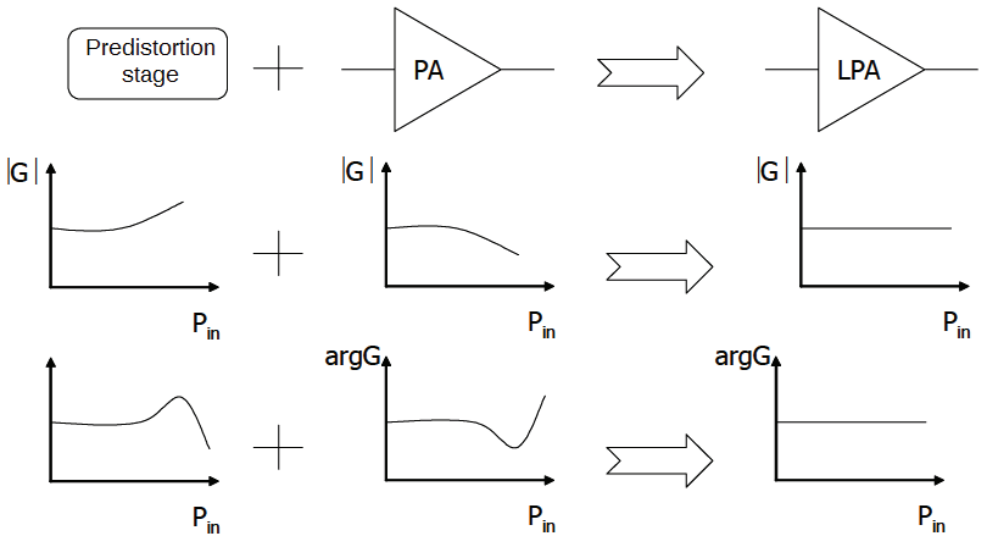


Figure 2.24: Principle of predistortion [17].

2.6.2 Closed Loop Strategies

Another manner to linearize a system is to create a feedback loop around it to generate an error signal that drives the direct path.

One possible strategy is to use polar loop. As it is possible to write a complex number in polar form, the transmitter is called polar because the information in amplitude and phase are treated separately as shown in Figure 2.25.

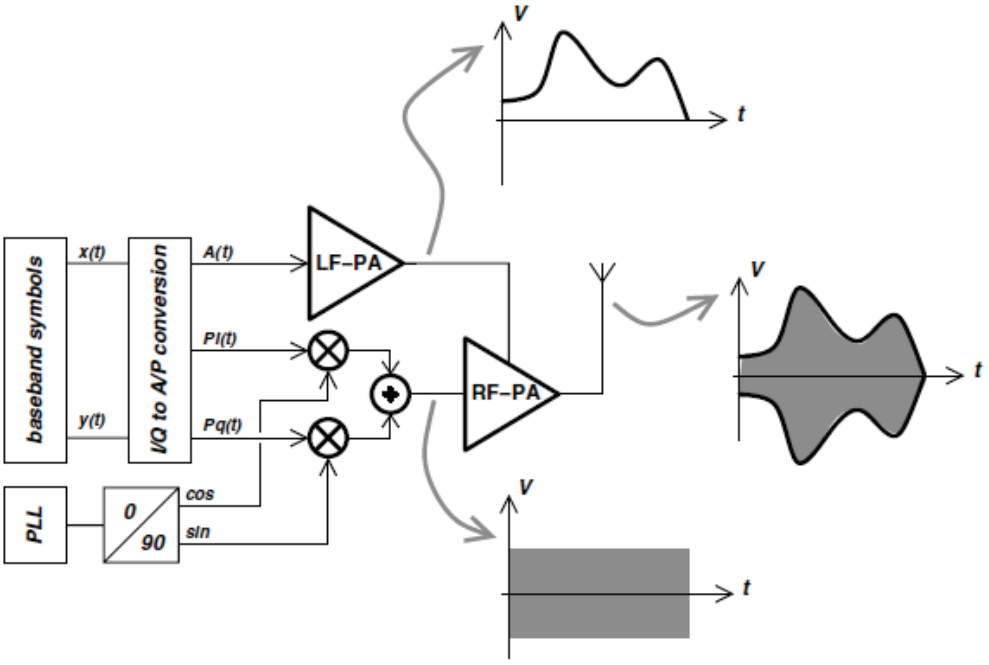


Figure 2.25: Polar loop architecture [56].

In this architecture, the baseband signals are translated from I and Q into amplitude and phase by

some circuitry, normally a CORDIC (COordinate Rotation DIgital Computer). The phase information is used to drive a high efficiency, non-linear power amplifier with constant power, so that the output power presents no dependence with respect to the input power. The amplitude information is used to drive a base band driver that controls the supply voltage of the RF power amplifier, obtaining amplitude modulation. Although the archtecture in Figure 2.25 presents no feedback, it is possible to imagine ways to obtain error signals to close the polar loop.

An important discussion is made in [57] about the correct use of polar loop. According to McCune, correct polar operation is only obtained when the power amplifier is used in compression, which makes the output power a weak function of the input power. This enables higher linearity to be achieved as it is discussed in Section 2.3.5.2. If the input power is not sufficient to drive the amplifier into compression, the technique would be called "Envelope Tracking" although the system schematics are similar. This technique has been largely reported [58][59] including patents [60][61] and a deeper discussion is beyond the scope of this text.

2.7 TECHNOLOGY ISSUES

In this work, a standard 130 nm CMOS technology HCMOS9GP from STMicroelectronics was used. The standard technology provides 6 copper metal layers, 1.2 V transistors with multiple V_{th} options (low leakage or high speed devices).

High voltage transistors (2.5 V and 3.3 V) are also available as process option. The modeled varactors use the 2.5 V option. In this work, ordinary MOS transistors were used as varactors due to cost issues.

In this work, the standard process was used due to cost issues. The output power of the presented circuits is limited by the technology robustness in the active devices but the techniques presented can be used in other technologies or process options without loss of generality.

For the sake of completeness, some discussion about passive devices is made here.

2.7.1 Integrated Capacitors

Capacitors are very important devices in RF design, being used in AC coupling, LC tanks and filtering. Therefore, it is essential to have good quality capacitors in order to achieve good performance. Normally, finger capacitors are offered in the standard process. In the used technology, these finger capacitors are called MOM capacitors and a top and side view is shown in Figure 2.26.

This kind of capacitor uses fringe capacitance among metal layers and, for that reason, the capacitance per area (capacitance density) is low. The capacitance density is basically limited but the minimum spacing the metal layers must keep in order to be correctly fabricated, as stated in DRC rules. One other drawback of this device is that the length of the finger should be minimized and the number of fingers should be maximized. This reduces the parasitic resistance affects the quality factor of the device.

Some IC processes offer MIM (metal-insulator-metal) capacitors as an option for the designer. As the

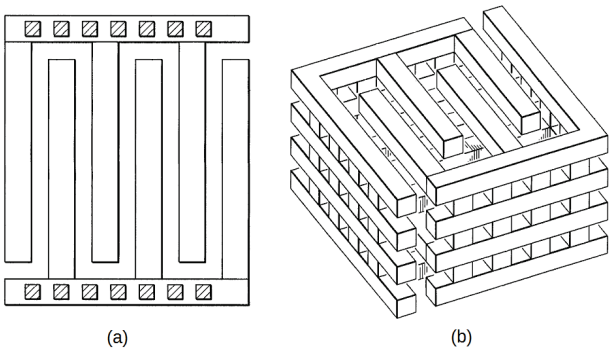


Figure 2.26: Finger capacitor: (a) top view and (b) 3D structure.

insulator can be made very thin in modern technologies, the distance between the two metal plates is kept small leading to a much denser capacitor. Moreover, the continuous metal plates present low resistance which leads to high quality factor. This type of device has the disadvantage of demanding additional process steps, increasing the cost of the whole chip.

A third type of capacitor is built from polysilicon layers. This kind of capacitor is very linear and they are also dense as the polysilicon plates are separate by a thin oxide. Despite these qualities, their use in RF design is not optimal as the sheet resistance of the polysilicon is orders of magnitude higher than metal stripes. This reduces the quality factor, which can also be understood as a high self RC constant. This kind of capacitor is widely used in low frequency analog design.

In this work, finger capacitors were used due to cost reasons. The quality factor of the finger capacitors, although important, is high enough for the application, presenting the order of magnitude of a few dozens.

2.7.2 Integrated Inductors

As well as capacitors, inductors are widely used in RF design, mainly in LC tanks and impedance matching networks. In RF design, there are basically two ways of implementing inductance: bondwires and planar inductors. As area is a critical aspect in IC design, these devices should be kept as small as possible as this is the strongest limitation on their use: the achievable values are fairly low, rarely reaching more than 15 nH at the expense of quality factor and self-resonating frequency.

Due to the range of frequencies of interest, in this text, the passives are modeled as lumped components simplifying the analysis [62]. In higher frequencies, this assumption fails and devices must be treated as distributed components and transmission lines.

In order to understand the use of bondwires and planar inductors, some electromagnetic effects must be discussed.

2.7.2.1 Skin Effect

Consider a conductor carrying current. In DC, the current flows uniformly across all the cross section of the conductor as shown in Figure 2.27. As the current frequency increases, the charge carriers has the

tendency to leave the core of the conductor and flow through the surface. This has the electrical effect of increasing the resistance of the conductor in large frequencies, therefore, increasing losses and decreasing the quality factor.

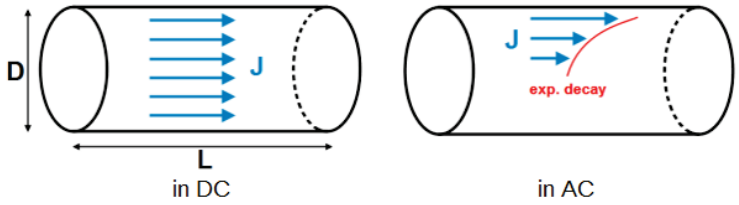


Figure 2.27: Skin Effect

In bondwires, this effect leads to current flowing through a cilidric AC conductor. Keeping in mind that bondwires are made of low resistivity materials, such as gold, the quality factor is kept high. On the other hand, in planar inductors, the current has the tendency to flow in the borders of the thin metal layers leading to high increase in the resistivity, as shown in Figure 2.28. For this reason, planar inductors suffer more from skin effect than bondwires.

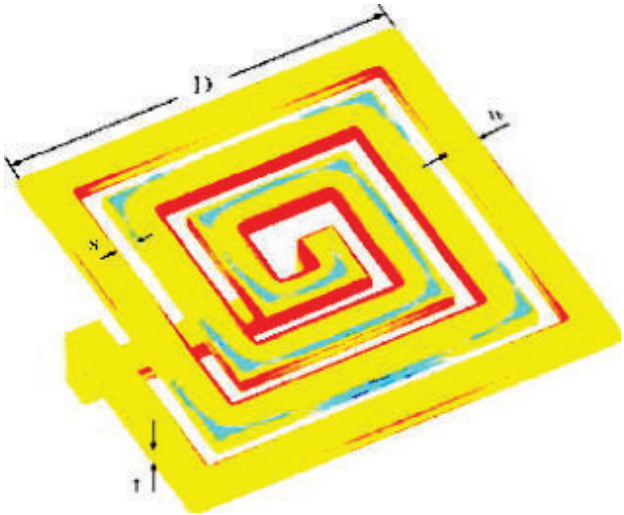


Figure 2.28: Skin Effect in planar inductors [63].

The shape of the planar inductor can also alter the electromagnetic characteristics. Some possible shapes are shwon in Figure 2.29. Circular inductors have a higher quality factor, as there are no corners for charge accumulation, but not all IC technology allows circular forms due to DRC rules. The octagonal shape is then preferred [64].

Futher informations and mathematical modeling of skin effect can be found in the literature [65][66][67].

2.7.2.2 Substrate Losses

The discussion about substrate losses only makes sense in planar inductors as bondwires are farther from the substrate and the electromagnetic field lines do not strongly couple with the substrate.

In CMOS technology, the substrate is normally P doped, which lowers the substrate resistivity. In

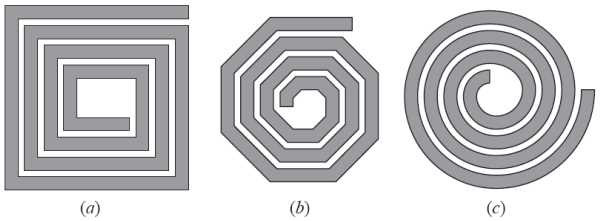


Figure 2.29: Planar inductor shapes.

modern CMOS, in order to avoid latch-up problems in digital circuits, the substrate is tends to be more heavily doped, reducing even further the resistivity.

When current flows in the inductor, the low resistivity collaborate to the existance of eddy currents in the substrate which increases the losses in the device as shown in Figure 2.30. In order to avoid this effect, a patterned shield is often used to prevent eddy current to circle over a large area [64]. Another way to alleviate these issues is to keep the coil as far as possible from the substrate, using top metals. This has an other advantage: as the top metal tends to be thicker, the series resistance of the inductor is minimized.

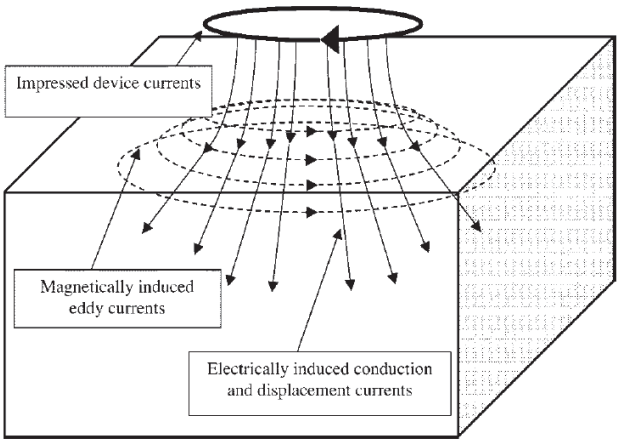


Figure 2.30: Electrically and magnetically induced currents [68].

2.7.2.3 Choice of the Device

The use of bondwires tend to be more expensive and more susceptible to process variations as the length of the wire is hard to control precisely on mass production.

For these reasons, planar inductors are widely used and were used in this work.

The used technology counts on RF addon module to provide several kind of modeled planar inductors built as p-cells. Inductor with only one turn present very low values, hundreds of picoHenry but very high quality factor and high self resonance frequency are available. On the other hand, wide metal inductors, capable of bearing very large currents with inductance values around a few nanoHenry and quality factor around 10 are also available.

3 METHODOLOGY

This chapter describes the methodologies used in this work. The used design flow will be discussed on Section 3.1 and the measurement procedures will be detailed in Section 3.2.

This work is part of a cooperation between University of Brasília, Brazil and University of Bordeaux, France, financed by Capes-Cofecub program in a regime of co-supervision. This PhD candidate spent 18 months in France where an important part of the design was made. The circuits are being measured by the french team due to delay in fabrication of the chips.

3.1 ANALOG INTEGRATED CIRCUIT DESIGN METHODOLOGY

The design flow of analog and RF integrated circuits are well known and, as any engineering design, start with a set of specifications both functional and electrical. Functional specifications are mainly related to the function of the circuit and some examples are amplification, multiplication, data type conversion, etc. Electrical specifications are related to the performances of these functions and some examples are power consumption, efficiency, gain, power supply rejection, etc.

A study on appropriate fabrication technologies is made in order to implement the desired function into hardware with the desired performance. Choices in this matter include discrete of-the-shelf components connected by PCB or integrated circuits. Integrated circuits can be fabricated using many techniques such as CMOS, III-V semiconductors, bipolar or BiCMOS to name a few. This work focuses on CMOS circuits due to its popularity and trend for integration of analog, RF and digital circuits on the same die, forming SoCs.

Given the choice of technology, the next step is to define the technology node to be used. As a general rule, smaller nodes are capable of achieving higher frequencies but are less robust to voltage stress. As another general rule, modern technologies provide more metal layers for interconnection and tend to present better quality factor of passive devices such as inductors.

The flow of mixed signal integrated circuits is shown in Figure 3.1. In this flow, the methodology for both analog and digital circuits is represented. The circuits designed in this work followed only the analog flow due to the characteristics of the circuits. The used digital circuitry was modeled in verilog behavioral level.

The design flow was made using Cadence Framework IC 5 with 130 nm STMicroelectronics standard CMOS. This technology provides 1.2 V transistor, 6 metal layers and native MOM capacitors. Process options such as high voltage devices and MIM capacitors are available but were not used.

The DRC (Design Rule Check) and LVS (Layout versus Schematic) verifications were made using Calibre from Mentor Graphics. All simulations were made in Cadence Spectre. Agilent ADS was not used due to incompatibilities with the design kit discovered in early design stages. ADS was not capable of

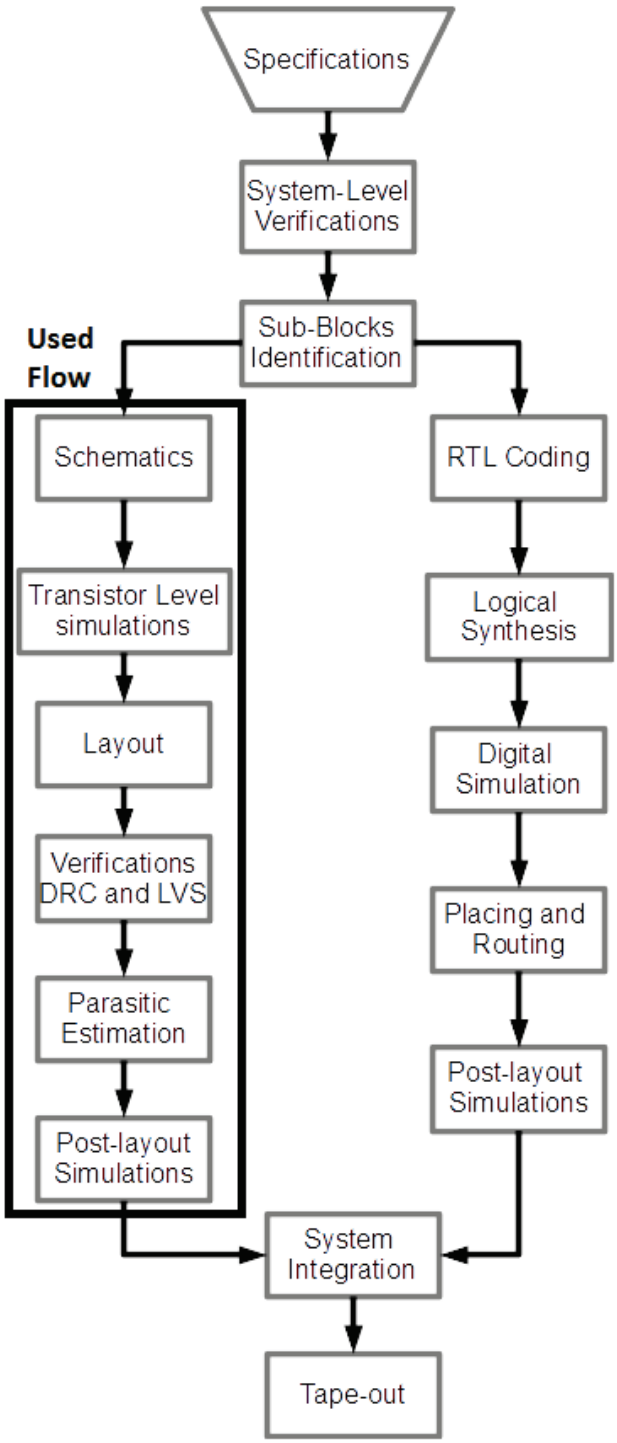


Figure 3.1: Mixed signal circuit design flow.

evaluating the transistor models of the design kit correctly.

The french team has a large experience in power amplifiers. In 2008, they have submitted a patent arguing for the power oscillator [69]. In this text, the idea of power oscillator is put. It uses a driver stage and a class E main power stage.

3.1.1 Design Methodology for a Power Amplifier

In this section, the methodology used to design the power amplifier is described.

The first design step is to evaluate the feasibility of possible solutions. Taking the topology proposed in [69] as a starting point, class E circuits were largely studied. In order to understand the circuit operation, ideal class E power amplifiers were designed using the design equations proposed by Sokal [29]. The ideal schematic is shown in Figure 3.2(a). Ideal reactive components and switch are provided in Cadence framework in analogLib. It is important to point out that the value of the load resistor in this stage was not set to 50 Ω as this would lead to a low output power, according to Equation 2.8, repeated here for convenience.

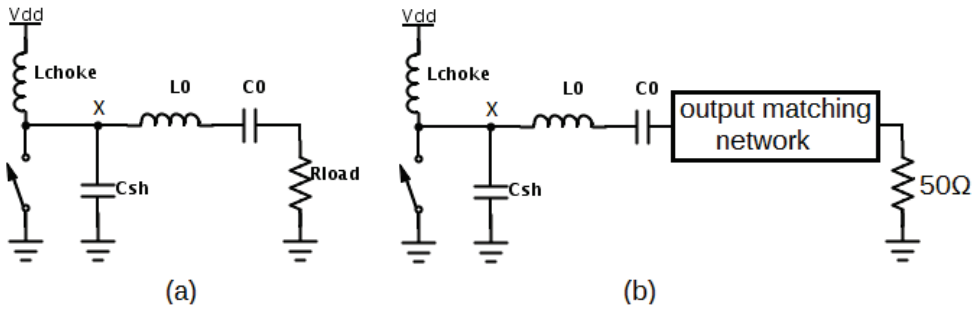


Figure 3.2: Ideal class E schematics.

$$P_{out} = k \cdot \frac{{V_{dd}}^2}{R_{load}} \tag{3.1}$$

Qualitatively, Figure 3.3 can be used to help the design. The voltage waveform is show in Figure 3.3 and the tendency of movement of this curve is shown. Aiming ZVS and ZdVS conditions, it is possible to correctly size the passive network.

There is a strong trade-off in sizing this load resistor. If it is made too large, the power will be reduced. On the other hand, it can not be made too small because the parasitic resistances of the interconnections will affect the implemented value, limiting the output power for a given supply voltage.

Once the value of the resistor is chosen, an ideal output matching network must be designed to translate the resistance into the chosen impedance of the circuit, in this case 50 Ω due to measurement issues. This design step is depicted in Figure 3.2(b). It is also important to remember that the losses in this transformation network grow with the impedance transformation ratio [24], in practical designs, also limiting the minimum resistance value and affecting both the output power and overall efficiency. ADS Smith Chart tool can be used to help in this process as nothing similar is present in Cadence Framework.

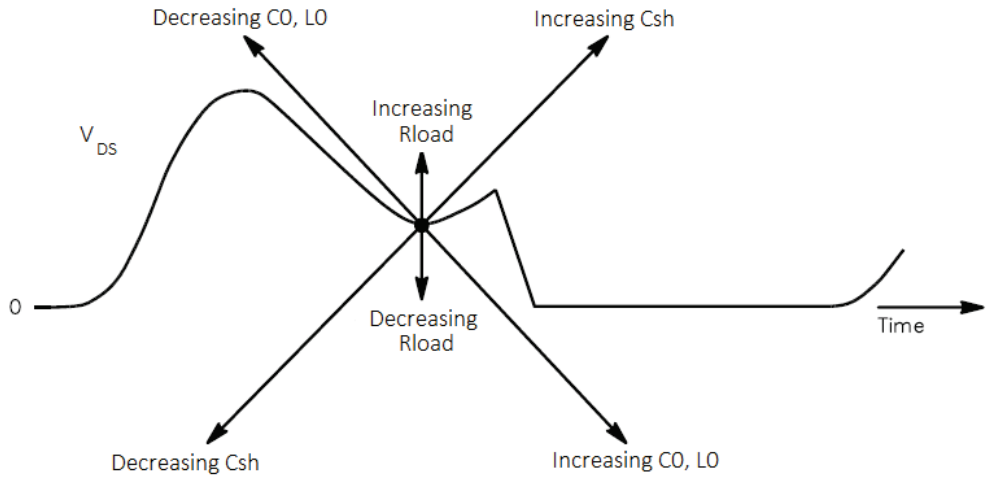


Figure 3.3: Effects of adjusting the load network [70].

Another aspect in this step concerns the input matching. As the ideal switch is driven by voltage, this initial model can not give any information on this issue. The goal of this initial model is to understand the behavior of the circuit and how voltage in node X in Figure 3.2 and current across the switch should be controlled.

In this design phase the problem with voltage stress already discussed in Chapter 2 was identified. As the voltage across the switch (implemented using standard transistors) would be too large, class E seemed not to be a good option for this design. As the issue was discovered in an early design phase, much effort and time was saved.

After some bibliographical research on how to deal with RF voltage stress and techniques to reduce it, the use of class EF2, presented in Figure 3.4, already discussed in Section 2.4, appeared as a good option. A new ideal circuit implementing an ideal class EF2 circuit was designed with the same goals:(i) analyze the behavior of the circuit according to theory, (ii) verify if the voltage stress issue was sufficiently alleviated.

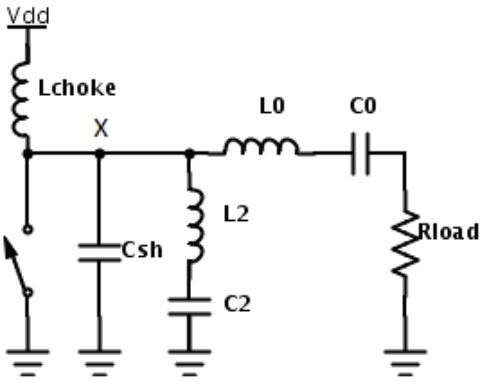


Figure 3.4: Class EF2 ideal schematic.

With a good result, the design passed on to a new stage: evaluating if the device sizes and values were feasible in the used technology and substitution of ideal devices for physical devices from the library one at a time to understand how each device's parasitics impacted the overall performance. It was noticed

that capacitors were very close from ideal devices and, therefore, were not critical. Inductors had a larger impact on efficiency and on output power due to higher parasitics. It is important to point out that each inductor was separately optimized in order to obtain the highest high quality possible given the amount of current they should tolerate. The inclusion of real transistors had the biggest impact on the performance and the size was designed to be a compromise between R_{on} and parasitic capacitance used in the waveform engineering of the voltage in node X.

With the inclusion of the transistor, the need for an input driver arose. This driver had mainly two functions: (i) drive the main stage with sufficient power and (ii) generate a driving signal with the correct duty cycle. The voltage signal generated by the driver should achieve its maximum around 1.2 V in order to minimize R_{on} and not overstress the main device's gate.

With the inclusion of the driver, the need for an input matching network arose. After the transistor sizing, the input impedance of the transistor was verified and an input matching network as designed to bring the transistor's impedance, mainly capacitive, to 50 Ω, also due to measurement issues.

In this moment, a first version of the class EF2 power amplifier was available using only components from the technology library. Final optimizations were made in order to maximize the efficiency and output power.

3.1.2 Design Methodology for a Power Oscillator

In this section the methodology used to design the power oscillator is described.

Being a power amplifier in a closed loop, much of the methodology used for the power amplifier can be reused. As the AM/AM characteristics of the power amplifier were known at this moment, it is possible to know how much power must be driven in the input of the power amplifier in order to obtain a certain amount of power. It was chosen an amount of power such that the amplifier would be compressed achieving maximum efficiency.

At this point, a systematic analysis should be made to fully understand the operation of the power amplifier. The circuit has no means to know which input power or driving signal is being applied as it operates in open loop. Imagine the designed power amplifier is compressed. In this situation, the transistor of the driver stage is biased in a certain manner and receives a certain $v_{gs_{AC}}$ (AC signal that drives the transistor) that is generated by the interaction of the power source and the input matching network. If one replaces the power source and the input matching network for a voltage source that generates the same bias condition and $v_{gs_{AC}}$, neither the output power nor the efficiency must not be affected in any manner.

Instead of using an ideal voltage source, a fraction of the output power can be used to generate an approximation of the $v_{gs_{AC}}$ that should drive the power amplifier. The bias point can be set using a biasing resistor. In this way, this signal generated from the output may be connected to the input, maintaining the circuit oscillation and generating a self-oscillating power amplifier.

This analysis may also contribute in further analysis such as phase noise. Assuming the mental experiment made above, the best case in phase noise comes from an ideal noiseless input. In this sense, only the direct path of the oscillator, i.e. the power amplifier, contributes with noise generation. This limits the

phase noise obtainable with power oscillators, no matter what is used in the feedback loop as it is dominated by the noise factor of the power amplifier itself. In this way, the use of high quality factor filters such as surface acustic waves (SAW) or bulk acustic waves (BAW) are limited by the power amplifier it self.

As conclusion, the design of a power oscillator follows the design of a power amplifier added the design of a feedback network that will be discussed now. It is not interesting to make the feedback in power mode as this would subtract much power from the output. As stated in the mental experiment, a feedback voltage should be generated to drive the input of the amplifier. The amount of power should, then, be minimized. Only sufficient power to keep the power amplifier in compression should be taken from the output. In this work, this feedback network was implemented using a capacitive voltage divider (responsible for controling the amount of power fedback) and an inductor for biasing and assuring phase conditions of Barkhausen Criteria. The schematic of the power oscillator is shown in Figure 3.6

3.2 MEASUREMENT PROCEDURES

This Section describes the measurement procedures adopted to obtain the results presented in Chapter 4.

3.2.1 Measurement of the Power Amplifier

As voltage stress is an issue in this circuit, the first test is supposed to be a robustness test. The goal is to establish if the circuit can hold the power levels in nominal biasing scheme.

For the power amplifier, shown in Figure 3.5, nominal biasing is:

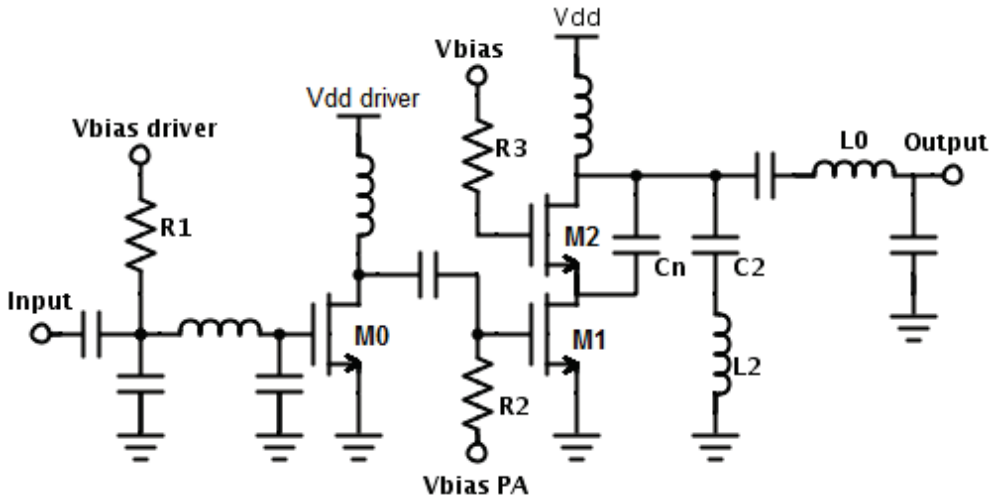


Figure 3.5: Schematic of the power amplifier

- Main supply voltage: 2 V
- Driver supply voltage: 0.8 V

- Bias voltage of the common-gate transistor: 2 V
- Bias voltage of the driver stage: 0.5 V
- Bias voltage of the common-source transistor: 0.35 V
- 50 Ω load

A complete discussion about the designed power amplifier is made in Chapter 4.

After applying nominal biasing with appropriate voltage sources, S parameters are measured with a network analyzer at very low input power level using 50 Ω terminations. All S parameters must be measured as these parameters will provide information about impedance matching and gain.

Spectrum analyzer, RF power sources and DC sources must be used to study AM/AM characteristics and output spectrum under different power levels also using 50 Ω terminations. Gain and efficiency (PAE and drain efficiency) can be extracted from this measurement. Varying the frequency of the RF power source will provide information about the bandwidth performance of the amplifier, always under 50 Ω terminations.

Finally, a load-pull measurement is made to measure how load variations can alter the efficiency and gain of the circuit for a given frequency. This technique consists of presenting different load impedances and evaluating the performance of the circuit on every presented impedance.

These procedures were made using a die and using probe stations. The cabling needed to build the setup is a strong source of parasitics and interference and the results may have been affected by the setup. The RF cabling was shielded but the DC cables are simple and grounding is a serious issue once several different equipment are used. Further improvements in the set up are being carried out.

A PCB is currently under development to provide more stable DC voltages and more capacitive decoupling to the setup. On-chip decoupling was added aiming to filter high frequency transients. Lower frequency transients, in the range of tens of MHz and lower, need to be filtered outside the die.

3.2.2 Measurement of the Power Oscillator

The test procedure is very similar to the ones described for the power amplifier and voltage stress is still an issue for the power oscillator. The same robustness test is made to identify if the circuit can hold the power levels under nominal biasing scheme.

For the power oscillator, shown in Figure 3.6, nominal biasing is:

- Main supply voltage: 2 V
- Driver supply voltage: 0.6 V
- Bias voltage of the common-gate transistor: 2 V
- Bias voltage of the driver stage: 0.5 V

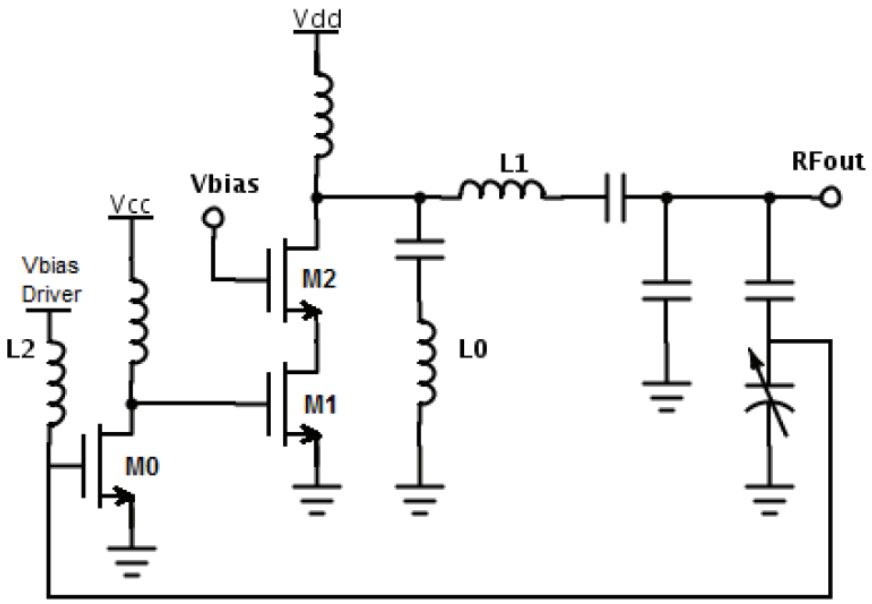


Figure 3.6: Schematic of the power amplifier

- Bias voltage of the common-source transistor: 0.35 V
- Control voltage must be between 0 and 1.2 V
- 50 Ω load

A complete discussion about the designed power oscillator is made in Chapter 4.

The small signal parameters are not possible to be measured due to the intrinsic large power generated by the oscillator.

A free-running test is made using DC sources and a spectrum analyzer with 50 Ω terminations. By altering the control voltage from 0 to 1.2 V it is possible to measure the voltage to frequency transfer function, DC power consumption and efficiency.

One important test to study the modulation capabilities of the circuit is the supply modulation test. It consists on altering the DC supply voltage and measuring the output power. It is important to notice that the circuit may not withstand oscillations if the supply is too low.

A load-pull measurement is also made in order to analyze how load variations can affect efficiency.

Finally, the phase noise must be measured using a spectrum analyzer. This test is very sensitive to input noise and shielded cables should be used.

These procedures were also made using a die and probe stations. A very similar setup was made for the oscillator. The same effects observed in the power amplifier were also observed in the oscillator: lower performances and low reproductibility which points to interference and parasitics introduced by the setup.

A PCB is also under development to provide more stable DC voltages and more capacitive decoupling to the setup. On-chip decoupling was also included for high frequency transients.

4 DESIGN AND RESULTS

In this chapter, the developed circuits and systems will be described along with the simulations and available measurement results.

As this work had the goal to study implementation and modulation of a power oscillator, this chapter starts by a high level model of an RF transmitter based on such circuit to study its technical viability.

In order to have a frequency specification, potential applications in 4G standard motivated the choice of the band around 2.5 GHz. This frequency is offered both in Brazil and in Europe [71] as part of the 4G band allocation and was chosen in order to provide results useful for both regions.

A high level modeling of the proposed solution is made in Section 4.1. This simulation is made to evaluate the viability and to give a crude notion on the expected performance.

The designed power amplifier will be presented in Section 4.2 as it is an important part of the proposed power oscillator. Discussions on voltage stress in switched power amplifiers will be made taking into account modern CMOS technologies. Simulation and measurement results will be shown for this circuit.

Using the results and experience given by the design of the mentioned power amplifier, the power oscillator, presented in Section 4.3 was designed adding to the PA a feedback network. Simulations and measurement results will also be shown. Aiming the next step of the project, a high level model of the power oscillator was generated and the model will be commented on subsection 4.4.

Comments of the integration of the complete solution in transistor level will be given in Section 4.5, closing this chapter.

4.1 HIGH LEVEL MODELING OF THE RF TRANSMITTER

Modern communication standards rely on complex modulations in order to obtain high data rates. The viability of the use of a power oscillator based transmitter in modern communication is studied in this section. As a complex modulated signal is modulated both in amplitude and phase, each characteristic is analysed separately.

Starting by analyzing the phase component of the modulated signal, and considering that a symbol is represented by the phase of the carrier in PM modulation schemes [72], the worst case symbol change include a 180° phase shift inside the window time frame of a symbol. This worst case is not uncommon as it happens in every bit change in a BPSK modulation, for instance.

Given the motivation, in order to achieve high data rates, the phase of the oscillator must be changed fast enough in order actually represent the desired symbol. This rises the question on the existence of a maximum phase shift an oscillator can provide when running on a given carrier frequency.

In order to simplify the problem but with no loss of generality, considering a voltage controlled oscilla-

tor with the following characteristics: constant gain over a certain bandwidth, limited range for the control voltage such as the one depicted in Figure 4.1.

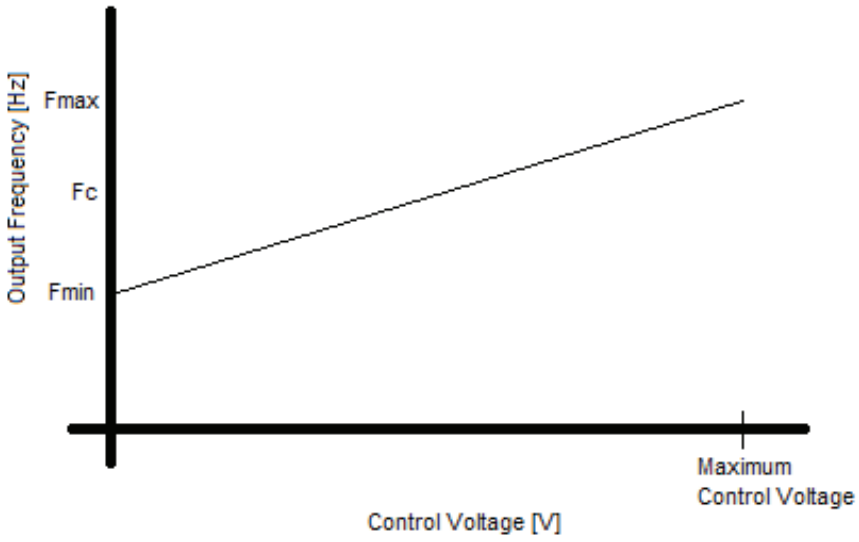


Figure 4.1: Transfer function of a linear VCO with limited tuning range

In order to analyse the phase control, some definitions are needed.

The VCO gain is defined as being:

$$K_{VCO} = \frac{df}{dV_{control}} \tag{4.1}$$

The VCO gain is used to establish a mathematical transfer function from the control voltage to output frequency. Most VCO exhibit a non-linear characteristic, which imply that K_{VCO} is a function of control voltage. In this text, the gain is considered to be constant and the conclusions are obtained without loss of generality.

Instantaneous frequency is defined by:

$$f = \frac{d\phi}{dt} \tag{4.2}$$

where ϕ represents the phase.

Using these definitions and Chain Rule from Calculus:

$$\frac{df}{dt} = \frac{df}{dV_{control}} \frac{dV_{control}}{dt} \tag{4.3}$$

The first term of Equation 4.3 can be recognized as the VCO gain and the second term is the variation of a voltage to the time inside the chip, which is limited by capacitances attached to the control voltage node. This states that frequency can not be changed instantly. As the control voltage is usually a base band signal, very fast frequency modulation is possible.

Now, phase modulation is studied. Once the VCO gain is defined, the output frequency is calculated

as:

$$f_{out} = \frac{d\phi}{dt} = K_{VCO} \cdot V_{control} + f_{min} \tag{4.4}$$

Equation 4.4 is the function depicted in Figure 4.1. The fastest phase variation is obtained when the oscillator operates at maximum frequency.

$$f_{MAX} = \frac{d\phi}{dt}_{MAX} = K_{VCO} \cdot V_{dd} + f_{min} \tag{4.5}$$

Similarly, the slowest phase variation is obtained at minimum frequency.

$$f_{MIN} = \frac{d\phi}{dt}_{MIN} = K_{VCO} \cdot 0 + f_{min} = f_{min} \tag{4.6}$$

As the oscillator is operating at carrier frequency, f_0, the phase shift responsible for modulation must be calculated relatively to this frequency. Defining:

$$f_0 = \frac{d\phi}{dt}_0 = K_{VCO}V_0 + f_{min} \tag{4.7}$$

Taking this into account, the maximum phase displacement from the carrier frequency is given by:

$$\frac{d\phi}{dt}_{MAX} - \frac{d\phi}{dt}_0 = K_{VCO}Vdd + f_{min} - (K_{VCO}V_0 + f_{min}) \tag{4.8}$$

$$\frac{d\phi}{dt}_{MAX} - \frac{d\phi}{dt}_0 = K_{VCO} \cdot (Vdd - V_0) \tag{4.9}$$

And similarly, the minimum phase displacement from the center frequency is given by:

$$\frac{d\phi}{dt}_{MIN} - \frac{d\phi}{dt}_0 = -K_{VCO}V_0 \tag{4.10}$$

Equations 4.9 and 4.10 state that there is a speed limit for phase modulation when the VCO is directly modulated. This speed is mainly dependent on:

- VCO gain: making the VCO gain very large is difficult due to the available varactors and may cause problems when close loop stability is needed, such as in a PLL.
- Tuning range: this range is often limited by the possible voltages a technology may sustain.

In the case of a non-linear K_{VCO}, as is most commonly the case, the VCO gain will be a function of the control voltage but will still be limited and, therefore, the qualitative conclusions presented still hold true.

Once the phase characteristics are described, amplitude issues will be discussed. As it has been pointed

out in Chapter 2, it is possible to modulate the amplitude of RF power amplifiers by modulating the supply voltage and this modulation should be very fast once a change in DC bias will rapidly reach the active devices due to low inductance feed that connects the supply voltage to the active device.

Bearing these two aspects in mind, a high level simulation of a polar transmitter was made in Agilent ADS. The simulated schematic is shown in Figure 4.2.

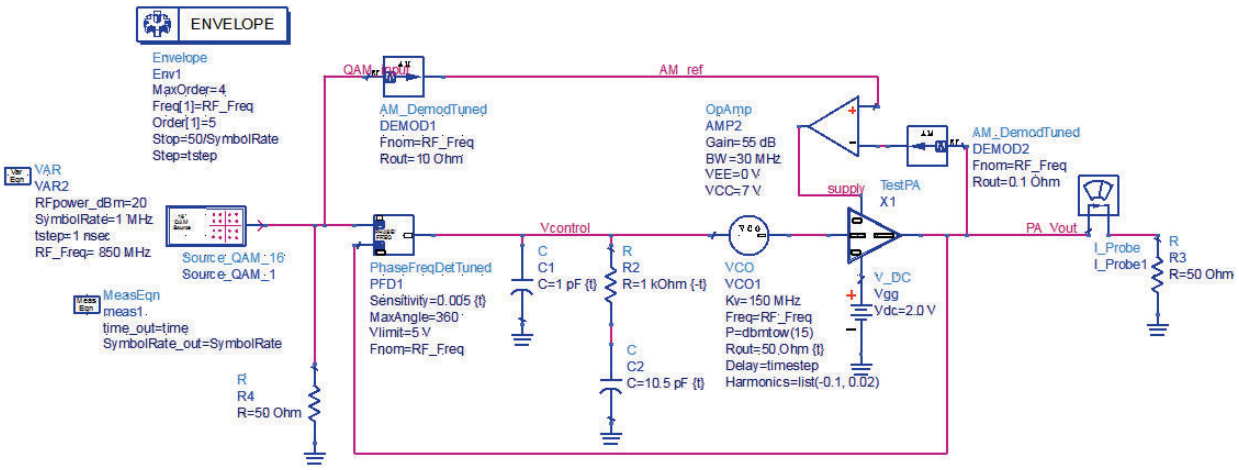


Figure 4.2: Schematic of the high level model of a polar transmitter

In this system, the power oscillator is modeled as a black box containing a linear VCO followed by a power amplifier. It is important to notice that the power amplifier is simulated in transistor level, adding parasitics and non-linearities that are typical of this kind of circuit. Also present in Figure 4.2 are:

- one 16-QAM source: this block generate random symbols modulated in 16-QAM with a controllable bandwidth.
- two AM demodulators: first demodulator is responsible for extracting the amplitude information from the 16-QAM source, presenting to the non-inverting input of the amplifier a base band signal that carries the amplitude information. The second demodulator has the same function with the output voltage.
- one baseband amplifier: this amplifier uses high feedback loop gain to make the output voltage follow the amplitude information of the 16-QAM source. It is important to notice that only baseband signals are presented to this amplifier.
- one phase-frequency detector (PFD): this block is responsible for comparing the phases and generating a feedback signal that makes the output phase follow the 16-QAM reference.
- a current meter.

It is possible to notice two separate feedback networks:

- one for phase control composed of a feedback that includes a classical type III PLL with a phase detector and a loop filter. The phase reference is given by a 16-QAM modulated signal. In this way,

the PLL phase should track the input reference. It is omitted in this circuit an attenuator responsible for reducing the power levels from the output of the power amplifier to levels that are bearable by internal digital circuitry. In physical implementations, this attenuator must be placed between the output node and the input of the PDF.

- one for amplitude control composed of a base band voltage follower. The envelope down-conversion is made by a linear AM demodulator block and a simple voltage amplifier makes the voltage envelope track the reference envelope generated by the 16-QAM source. It is omitted in this model the circuits that will be responsible for delivering large currents, such as an LDO. In order to be able to omit this circuit the output impedance of the used amplifier is made very low, allowing it to deliver large currents with low voltage drops.

Simulation results for amplitude modulation are shown in Figure 4.3. The waveform on top of Figure 4.3 present the baseband voltage amplitude of the reference 16-QAM source in volts and the error calculated between the reference and output amplitudes is shown in the bottom of Figure 4.3. Simulation results for phase modulation are presented in 4.4. Similarly, the phase of the reference 16-QAM souce is shown on top of Figure 4.4 in degrees, and the phase error between reference and output is shown below.

It can be noticed in Figure 4.3 that after an initial stabilization period the error is kept close to zero along the whole simulation, indicating that the envelope of the output signal follows the input at that data rate. The achievable speed will be dependent on the bandwidth of the feedback network.

The PA input signal is simulated to be around 850 MHz and a passband simulation is used in order to be able to simulate the PA in transistor level. The PA was chosen from a library inside ADS and had been optimized for 850 MHz. This avoids the need of design of a PA and can be used to prove the viability of the idea. It is known that power amplifiers introduce some phase distortion but it can be seen that, as the PA is inside the PLL, these distortions are corrected by the loop. The PA used was taken from a design example from ADS and is used in compression region, to obtain higher efficiency. According to the theory involved [57], in order to be able to modulate the amplitude of the PA by the supply voltage, the PA must be driven to saturation. This would be explained by the fact that, when compressed, the output power is no longer a strong function of the input power, leaving the output power only dependent on the supply voltage.

One drawback of this architecture, though, is the achievable data rate in the PM path. As the PLL is composed by a low pass filter (composed by C1, C2 and R2), the output phase tends to the reference in a fairly slow pace. Speed can be traded off with accuracy of the loop once this filter is responsible for eliminating transient glitches. The lock time being fairly large, around of hundreds of microseconds, the data rate would be limited to some thousands of symbols per second. As the filter is much slower than the limitation of the VCO, presented previously, the VCO is not responsible for this behavior described previously.

It can be noticed that both the amplitude and phase error are kept low after a settling time. Glitches in phase errors are observed due to 180° change but the system rapidly achieves lock state.

In order to evaluate quality of modulation RF parameters, the modulted constelation in shown in Figure 4.5 and the output spectrum is shown in Figure 4.6

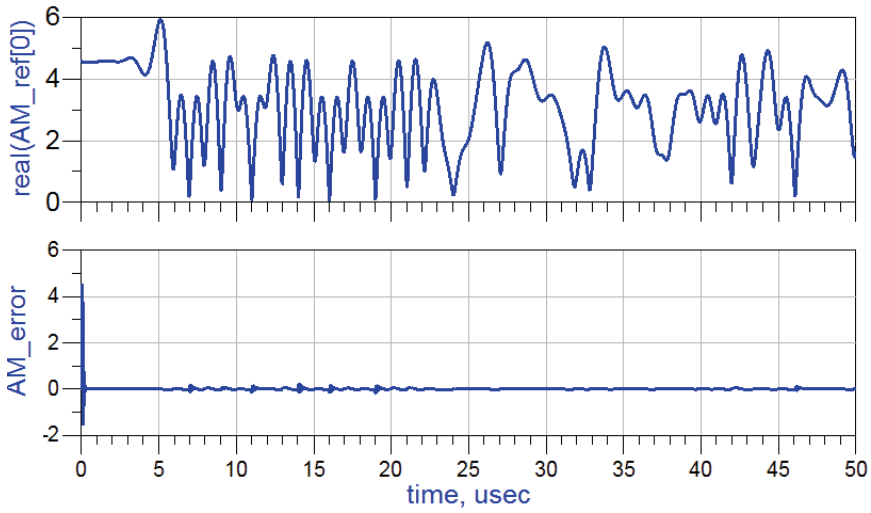


Figure 4.3: Simulation results for amplitude modulation.

The 16-QAM modulation constellation can be observed in Figure 4.5 without noticeable distortion.

In the spectrum, the input signal, shown in blue, was generated using two random bit generators that are used to modulate a carrier. The bit waveform is filtered in order to select only the main spectrum lobe, otherwise the bandwidth of the modulated signal would be infinite.

It can be seen that the output signal follows the input signal with added noise, as would be expected. The power in adjacent channels, measured by ACPR (adjacent channel power ratio), is more than 40 dBc and would be sufficient for many communication standards [73].

As it can be noticed, no constraints are kept on the reference signal. Once it is possible to generate a reference signal, the transmitter should be able to deal with it once the speed limitations are respected. This fact make this transmitter very versatile and reconfigurable.

These results validate the technical viability of the solution but discourage the use of this topology for high throughput transmission schemes. Next step would be to implement the RF circuits in silicon and the implementation will be discussed in the following Sections.

4.2 POWER AMPLIFIER DESIGN AND RESULTS

As the power oscillator is mainly composed by a power amplifier, it is important to obtain interesting characteristics in the power amplifier before designing the oscillator. First important characteristic is to obtain high efficiency as the power amplifier is often the most power hungry circuit of the RF transceiver. This need points to the use of switching-mode power amplifiers such as Class E. Due to the discussion on voltage stress made in Chapter 2, Class EF2 was chosen to be used in the main power stage. This class of operation had never been presented neither in RF frequencies nor in standard CMOS technology. As the main power stage must receive a square-like voltage waveform to control the switch, a conformation stage is need, since the input signal is nearly a sinusoidal.

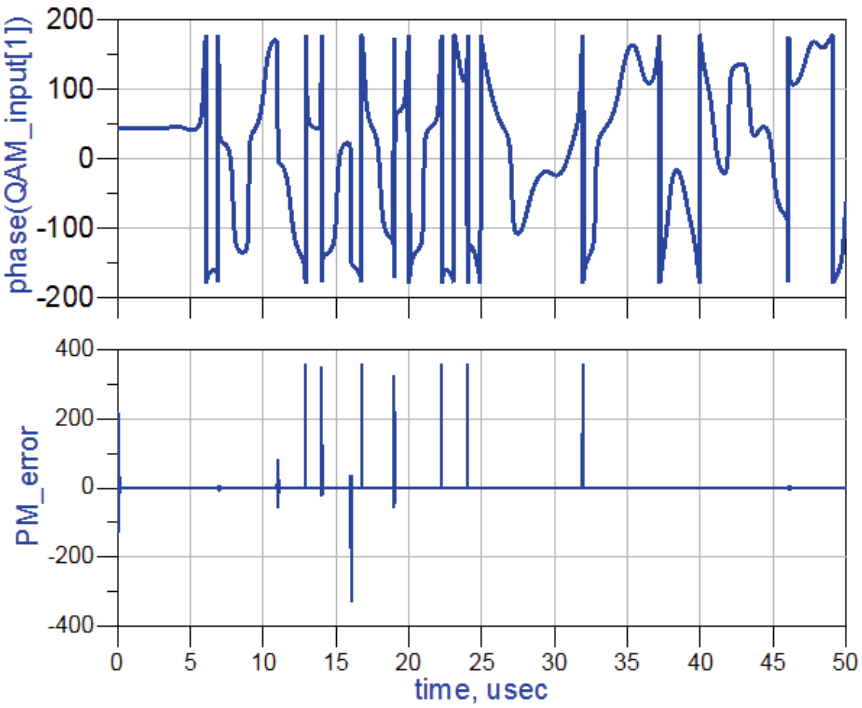


Figure 4.4: Simulation results for phase modulation.

Possibilities for the driver stage are commented below. Works that use no conformation stage have also been found [46] but as it contradicts the operation theory of the switching circuits, this option was not taken into consideration.

1. Diode based. A diode is used to short circuit half of the sinusoidal waveform to present the square-like voltage to the switch. This approach has been used in [45] and [37]. This passive approach leaves all the power gain to the main stage. As a consequence, the obtained efficiency is lower.

2. Push pull. The push-pull CMOS amplifier can be used to deliver a square-like voltage waveform. The large input capacitance of the main stage represents a difficulty to this topology that presents high output impedance. In this way, the driver transistors must be made very large in order to deliver enough current. Intermediate simulated efficiencies have been observed with this driver.

3. Sinusoidal driver. A common-source amplifier with an inductive load can be used as a driver if the transistor is appropriately sized, in order to present low on resistance. Due to the operating point of the drain, be ideally the same of the inductance DC biasing, a lower supply can be used. Low inductance values also reduce the output impedance of the driver making it able to deliver large currents from a low voltage supply. Higher efficiencies were observed at the expense of the surface for an inductor.

As a consequence of the analysis previously made and the search for high-efficiency, circuits a sinusoidal driver was chosen. The biasing is such that it controls the duty cycle of the main stage, and so, it can vary between class AB to class C.

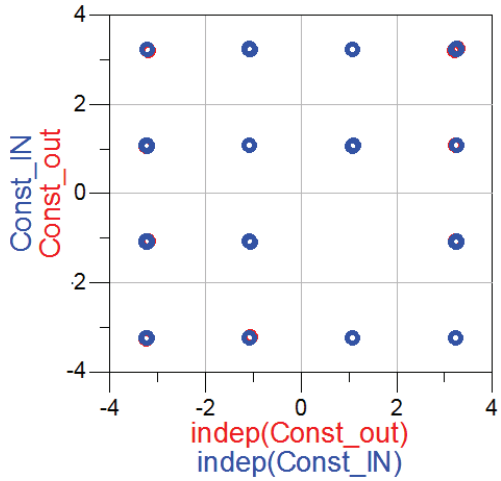


Figure 4.5: Simulated constellation.

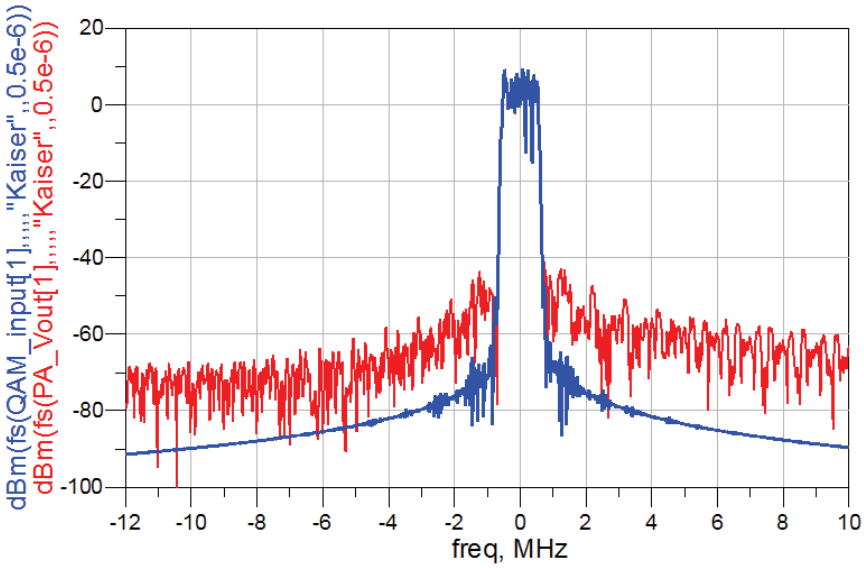


Figure 4.6: Simulated input and output spectrum.

As it can be seen in Figure 4.7, the designed power amplifier is composed of an input matching network, a driver stage and a main stage. Each of these parts will be discussed in further details.

As transistors M1 and M2 must be capable of driving large peak currents, they are made very large. Their size brings non-negligible parasitic capacitance. Some parasitic capacitance of M2 is used to implement C_{sh} of Figure 2.15 from Chapter 2. The parasitics electrically connected to the drain of M1 in Figure 4.7 degrade the efficiency as it delays the voltage at that point, causing overlap between voltage and current.

Suppose all parasitic capacitance can be modeled as C_P in Figure 4.8. The addition of C_n uses Miller effect to implement a negative capacitance that is used to remove the parasitics as shown in Figure 4.8, where K is the voltage gain of the common gate stage, that is positive [35][36]. Efficiency gains such as 6% are described and a comparable gain in efficiency was observed in the designed circuits.

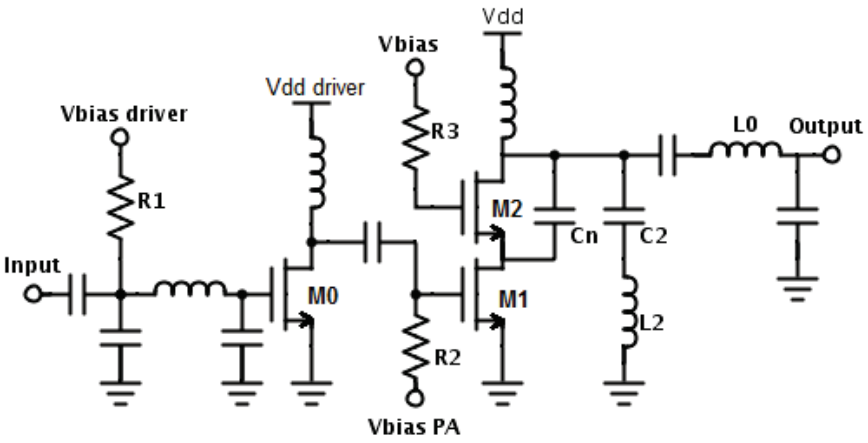


Figure 4.7: Schematic of the power amplifier

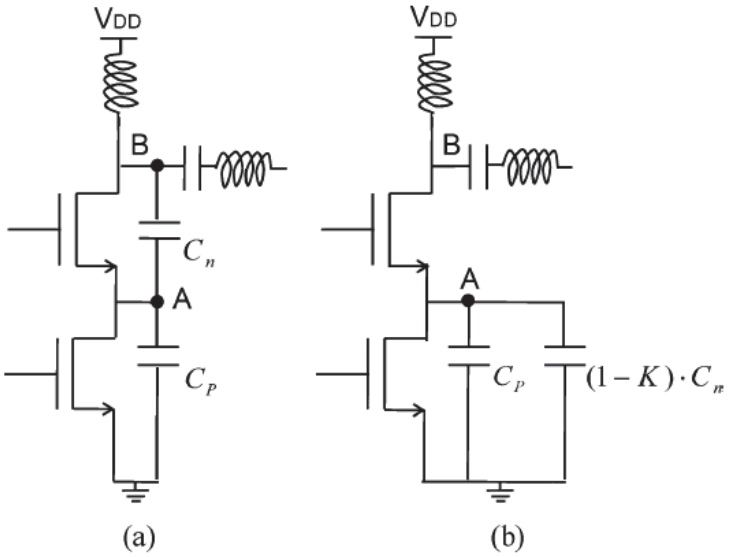


Figure 4.8: Negative capacitance implementation[35].

The addition of C_n can be seen as positive feedback and potentially lead to unstable behavior. As the transistor size is large, the transconductance is large, leading to large voltage gain. Therefore very small capacitance values are used to eliminate the parasitics and reducing the risk of instability [35][36]. Resonating the parasitic capacitance has also been proposed [32] but this solution increases area, provides a narrow band solution that is very dependent on the quality factor of the used inductor.

All used inductors were taken from a library and designed to present a quality factor as high as possible, rarely lower than 10, around the frequencies of interest. In the case of the inductor marked as L2, the quality factor was optimized to frequencies around 5GHz as the series LC tank should implement a short circuit around that frequency. Due to the high current that must go through L0, a large metal width was used.

4.2.1 Input Matching Network and Driver Stage

The input network is a π network responsible to change the transistor's input impedance into a desired one. In this circuit, the input matching was made to 50 Ω in order to perform an easy connection with the measurement equipment. The Agilent ADS was used to design the input network. The transistor's input impedance was simulated using Cadence Spectre and the value was used in ADS. Notice that ADS could only deal with simple models for the passives. In the case of the inductance, only resistive losses could be modelled. This led to further design work in Cadence in order to obtain an adequate matching circuit.

Once the power is delivered from the source to the PA through the input matching network, the driver is responsible for:

1. Some power gain: once the transistor of the main stage is much larger, enough power must be delivered. This is accomplished by a low drain impedance, which is able to deliver large AC currents to the capacitive load and, therefore, enable fast switching of the main transistor. High quality factors for the drain inductance were mandatory to a good performance, once ohmic losses are present in the inductance. Due to these losses, the DC biasing of the main stage cannot be accurately established through the inductance and a capacitive coupling was included.

2. Waveform conformation: As the main power transistor is expected to switch, for good operation, a square-like voltage waveform drive its gate, given its source is grounded. The choice of the supply voltage should be made with the choice of drain inductance, once they control the peak voltage value. Higher supply voltages will often lead to higher efficiencies but they may overstress the main transistor, leading to breakdown. Grounding issues will be discussed elsewhere. As will also be discussed later, the control upon the duty cycle of the voltage waveform that controls the main stage is essential to obtain some characteristics. This control is made by altering the DC bias point of the driver, given that the driver transistor will turn on earlier or later, leading to different conduction angles.

4.2.2 Main Power Stage

Transistor size represent a trade off between R_{on} and input capacitance. Cascode structure was used to split the voltage stress. Transistor sizing was optimized for optimal time domain waveforms and efficiency. Based on simulations of amplifier with ideal components, inductor values and track widths were estimated. These initial parameters were optimized in simulation for the efficiency and current handling capabilities. Finally, an L network was designed to alter the virtual load into 50 Ω for physical measurement.

Some stability precautions must be discussed. Special care must be taken with DC biasing. The direct connection by a metal track to the DC pad implement a parasitic inductance that can lead to instability, mainly due to the large voltage gain of the devices. Resistors R1, R2 and R3 are used to present a dominantly resistive impedance to the gates of M0, M1 and M2, respectively in Figure 4.7.

Another important measure is to add decoupling capacitors wherever it is possible. Omitted for simplicity, the node connected to the gate of M2 is decoupled forming a low pass filter that avoids oscillations

at that node. All DC inputs are decoupled with at least 20 pF. For the supply voltage of the main stage a total capacitance around 70 pF was used without increase of silicon area.

The DC value of Vbias is also important to be discussed in detail. This voltage controls the maximum voltage stress M1 will be subjected to. This happens because as the V_{S2} rises, V_{GS2} is reduced, eventually, turning M2 off. From that moment on, all voltage is held by M2 as the impedance presented by M2 is higher. The value of this voltage should be as high as possible as it reduces the R_{ON} of M2, reducing the power losses. A clear tradeoff between efficiency and robustness is presented. The correct biasing of the cascode switch is not only essential for efficiency and power but also to guarantee the lifetime of the circuit.

The maximum voltage stress presented to M2 is dependent of the supply voltage. The supply voltage is directly related to the output power but may cause overstress on the devices, hence, presenting another clear tradeoff. Because of these issues, both the supply voltage and the biasing conditions must be chosen carefully to assure the circuit will work properly and efficiently.

As it is known, the final step in the design of analog circuits include the extraction of parasitics from layout and the circuit re-simulation in order to evaluate the impact on the performance. Due to the large computational power needed to estimate parasitic inductance, the tools provide resistive and capacitive parasitics more often. The so called “RCc extraction” estimates the parasitic resisitances and capacitances both coupled and decoupled. This was the type of extraction that was made for the power amplifier and power oscillator.

The model generated after parasitic estimation for the class EF2 power amplifier was simulated with a source degeneration inductance to understand how this circuit would behave during measurements. This dependence is shown in Figure 4.9. It can be noticed that very small values of parasitic inductance have strong influence on the output power and power gain. Once both output power and gain are reduced by these parasitics, the efficiency will be surely jeopardized.

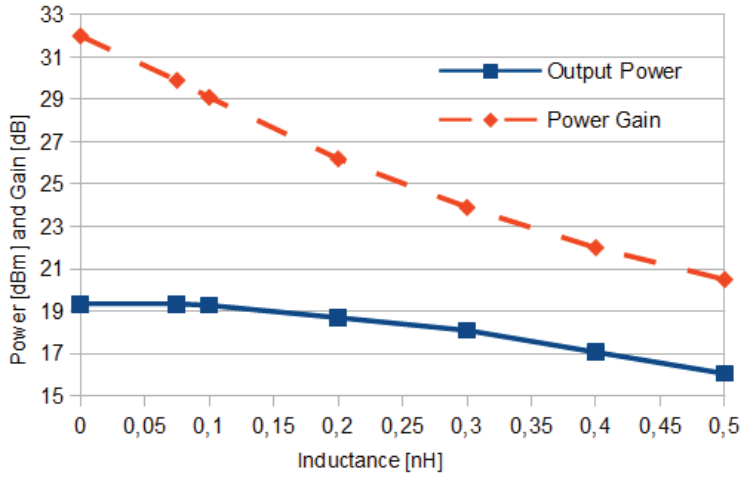


Figure 4.9: Dependence of output power and power gain over source degenerating parasitic inductance.

In order to reduce the parasitic inductance present in the source of the power amplifier, a ground plane was made. This ground plane has the goal to present many parallel paths to current to ground, reducing

the ground resistance but, more importantly, also inductance. The ground plane was designed in a way that all layer densities were fulfilled just by its existence, from polysilicon to metal 6. In this way, the ground plane was taken to every empty part of the chip. The ground plane was not taken into the exclusion zones of the inductors. Figure 4.10 present the layout of the ground plane separate layer by layer. Using all metal layers, the number of parallel paths to ground is maximized, minimizing the inductance. All layers are connected through vias.

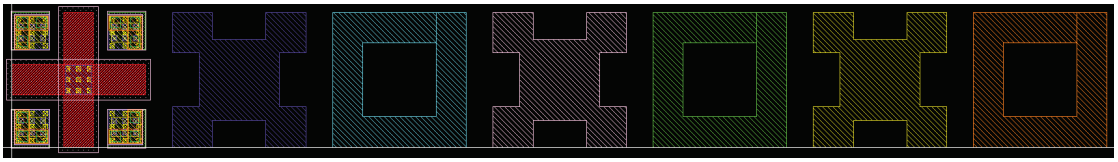


Figure 4.10: Ground plane cell from polysilicon to metal 6.

Also in order to reduce the parasitic inductance, as many ground pads as possible were added to the chip and connected to the ground plane. This procedure potentially reduces the impedance out of the chip.

The same cares were taken with the power oscillator once the two circuits operate in a very similar fashion.

4.2.3 Power Amplifier Simulation and Measurement Results

The micrograph of the prototyped power amplifier is shown in Figure 4.11. The main difference between the PA and the oscillator is the position of the driver stage and the main stage. In the oscillator the driver is closer to the output to enable the feedback with a small connection, avoiding parasitics. The circuit occupied 1660 μm x 1470 μm including pads in standard 130 nm STMicroelectronics technology. This technology provides 1.2 V transistors and 6 metal layers.

In order to guarantee minimum overlap between voltage and current in the power device assuring the correct voltage waveforms, an intensive simulation process was used and the goals was to achieve highest power and efficiency possible.

The simulated current and voltage waveforms are presented in Figure 4.12. It is known that keeping the transient voltage stress below two times the nominal supply voltage will not damage the devices or reduce its lifetime significantly [32]. It can be noticed that the drain voltages are kept below 2 V due to the choice of both supply voltage and the biasing of the common-gate transistor. It can also be noticed the small overlap between voltage and current, assuring correct operation.

The first parameters measured for this circuit were the small signal S parameters. The small signal S parameters were simulated with a -40 dBm input power. A small signal power gain of 32 dB was expected and the input matching is satisfactory as it can be seen in Figure 4.13.

Following the same guidelines, the circuit was measured using a network analyser in IMS laboratory with the same -40 dBm input power. All power sources present 50 Ω. The measurements can be seen in Figure 4.14.

It can be noticed the gain, represented by S21, is 3 dB lower than simulations. The same behavior is

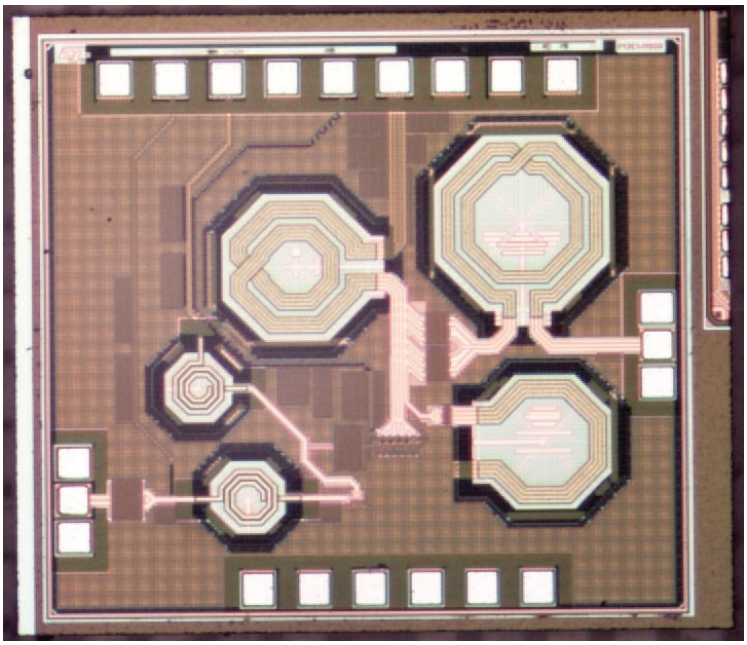


Figure 4.11: Micrograph of the prototyped class EF2 power amplifier

observed in the input matching, S11, that is slightly higher. Strong differences are observed in S22 and this may have strong impact on the efficiency once the correct impedance must be presented to the drain of the current switch in order for the voltage and current waveforms to behave as predicted in EF2 class. As the inductance feed is not high enough to be considered a choke, non idealities in the voltage supply net may alter this parameter. It is very difficult to conclude the problem to be on the circuit once S11 and S21 are reasonably close to simulation. One way to evaluate this possibility would be to add further decoupling to the supply lines in a PCB for example.

Following the small signal S parameters, large signal measurements were made. One very clear characteristic of a class EF2 power circuit is the generated spectrum. The expected spectrum is shown in Figure 4.15 under nominal operating conditions. Under full power operation (0 dBm input power), the circuit consumed 192.6 mW for the class EF2 power amplifier and the driver at 2.5 GHz.

It is clear that the 2nd harmonic is 16 dB weaker than 3rd harmonic. This characteristic is given by the short to the 2nd harmonic across the switch. The screen of the spectrum analyser used for large signal measurement is shown in Figure 4.16.

As it was expected from the small signal measurements, as the gain dropped, the maximum output power is reduced to 15.89 dBm. The power difference between the 2nd and 3rd harmonic was also influenced. In measurement, the 2nd harmonic is lower as expected but only 12 dB. The reason to this variation could be the variation of the impedance seen by the drain of the power transistor and reflected in S22.

The simulated AM/AM conversion characteristic referred to 50 Ω impedance for input and output is shown in Figure 4.17. Due to the 32.7 dB power gain that is observed and the 2 V supply voltage, the output compression point is found to be 9.1 dBm.

As it can be seen the power amplifier should be able to reach 20 dBm under nominal operation condi-

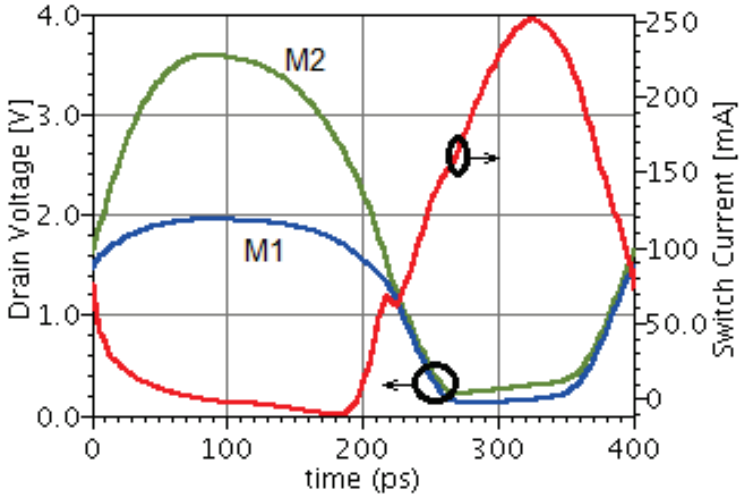


Figure 4.12: Simulated current and voltage waveforms in the class EF2 power amplifier.

tions. The measurements for these characteristics can be seen in Figure 4.18.

Very differently from simulations, the power amplifier is not compressed with -20 dBm input power. This can be seen by the flatness of the power gain curve for input power lower than -18 dBm in Figure 4.18. In simulation, the power amplifier starts to compress around -30 dBm.

Efficiency has also been affected. Figure 4.19 depicts the simulated results. The drain efficiency (DE) reaches 55% while power-added-efficiency (PAE) reaches 50%. It can be observed that the two curves split gradually as the input power increases. This happens because the input power is subtracted in PAE and the power consumed by the driver stage also increases.

The efficiency measurements are shown in Figure 4.20. It can be seen that both DE and PAE are reduced. It can also be seen that DE has suffered a larger degradation as the two curves follow almost toghether until very high input power levels. This observation is also in accordance with the discussion about S22 made earlier.

The shape of the curves are also affected. For small input power levels, the degradation is around 1.5% of both PAE and DE. As input power increases, the curves get compressed. This point to an incorrect class EF2 operation where the overlap between voltage and current is not observed. The reason for this is also variation of the impedance presented at the drain of the power transistor.

The output power, PAE and drain efficiency (DE) with a wide variation of frequency is shown in Figure 4.21, while the input power is kept 3 dBm. The presented circuit is able to work from 1.5 GHz up to 3 GHz if the 3 dB power drop criterion is observed. It should be noted that the efficiency of the PA is sacrificed if full span is used. On the other hand, if efficiency must be kept high, PAE varies 2.5% while the DE varies only 1.6% among 2.1 GHz and 2.6 GHz. It provides a 500 MHz high efficiency bandwidth, in which the output power varies only 0.6 dB. This can be obtained since the passive network characteristic is such that the non-overlapping condition is maintained. It can also be noted that, as DE is kept constant over a wider range, the driver is responsible for some degradation. The bandwidth in which the output power degrades 1 dB (1 dB output power bandwidth) is found to be 28.2%. The same value was found for the bandwidth

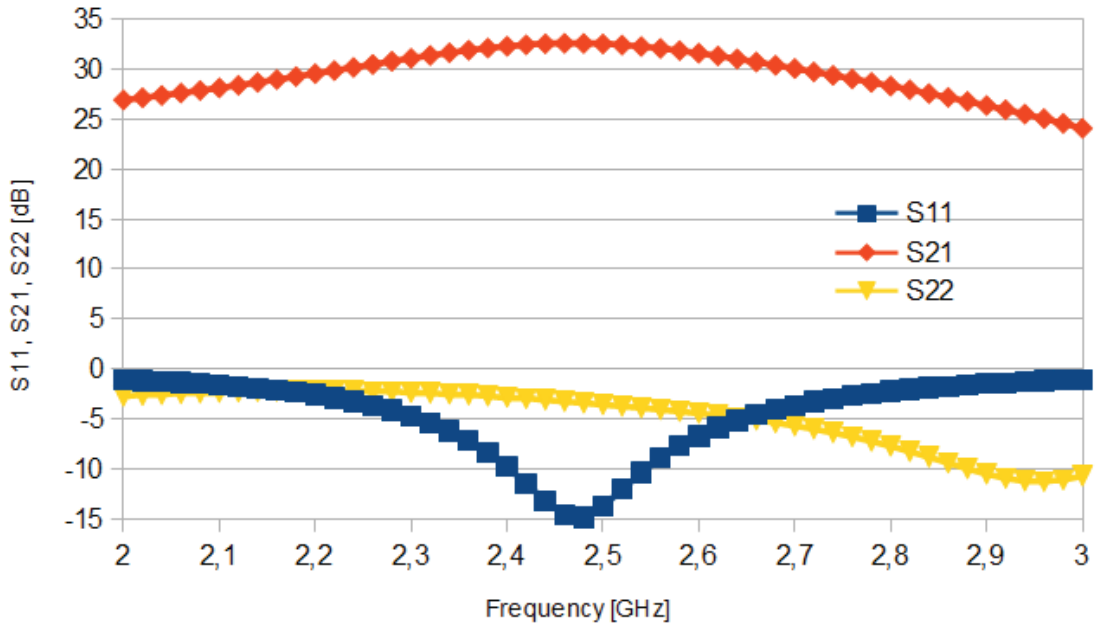


Figure 4.13: Simulated small signal S parameters

in which the PAE falls 3% (3% PAE bandwidth).

The measured results are presented in Figures 4.22 and 4.23. The large bandwidth characteristic is maintained despite the drop in efficiency and output power. In fact, the output power is more flat in measurement. The 3dB bandwidth starts in 1.8 GHz and goes up to 3.4 GHz. The 1 dB bandwidth measured is 38% (2.15 GHz to 3.1 GHz).

The shape of the curves have been affected and the flatness in efficiency is not present in measurement. The -3% PAE bandwidth is found to be 26% against 28.2% in simulation. This result shows the circuit is still capable of operating over a large bandwidth. The large bandwidth allows the use of the same hardware in different communication standards such as Bluetooth, Wi-Fi, ISM band as well as the 4G band initially aimed.

The former 5% difference between DE and PAE has been reduced to 2.5% and this evidence also points the drop in the achieved DE as noticed earlier in this section.

For the sake of comparison, Table 4.2.3 presents the features of some switched-mode power amplifier. All values for this work in Table 4.2.3 are post-layout simulations.

To the author's knowledge, this is the first time the waveform engineering present in class EF2 is used in RF frequencies. It can be noticed that almost all class E PA use high voltage transistors in order to address the high voltage stress. Cascode switches are also very common. The amplifier presented in [32] achieves high efficiency as all inductors are implemented using bondwires. The work [40] also uses bondwires to implement inductors. In [33], due to the low power output, native transistor are capable of dealing with the voltage stress and high voltage transistors are not needed. The designed circuit presents PAE comparable with the other circuit without the use of any process option while delivering power in the range of hundreds of miliwatts. This was only possible due to the use of class EF2.

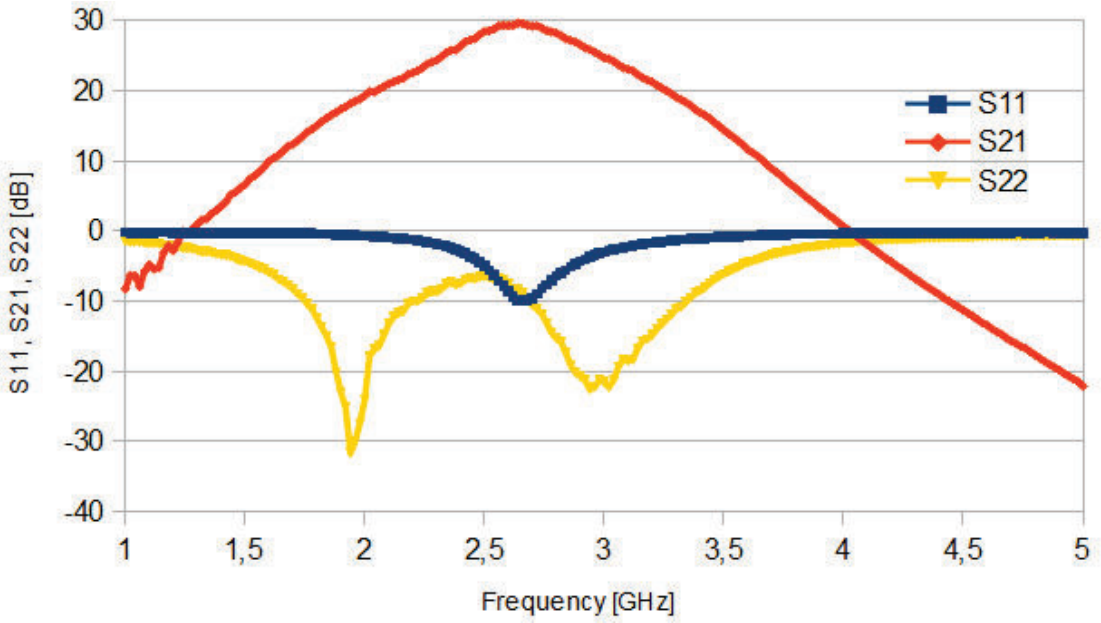


Figure 4.14: Measured small signal S parameters

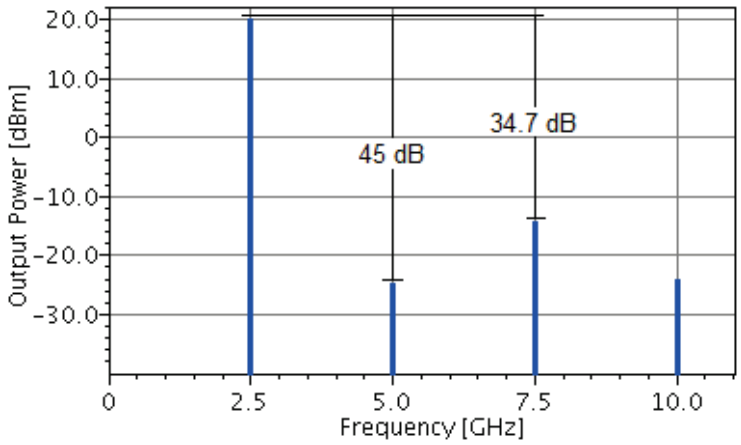


Figure 4.15: Simulated spectrum for the class EF2 power amplifier.

It is clear that the performance of the circuit in terms of power and efficiency has been affected by measurement. A potential reason is the variation of the impedance seen by the drain of the power stage in measurement. This can be seen by the variations of S22. One other possible source of degradation is the inductive source degeneration. The large bandwidth capability shown by the circuit, in the author's opinion, reinforce that the measured degradation is a result of the setup and can be improved by further decoupling and using a PCB to feed the DC voltages into the circuit.

4.3 POWER OSCILLATOR DESIGN

This section continues the discussion on the simulation and measurement taking into account the class EF2 power oscillator. The schematic is shown in Figure 4.24. The discussion about the inductive parasitics

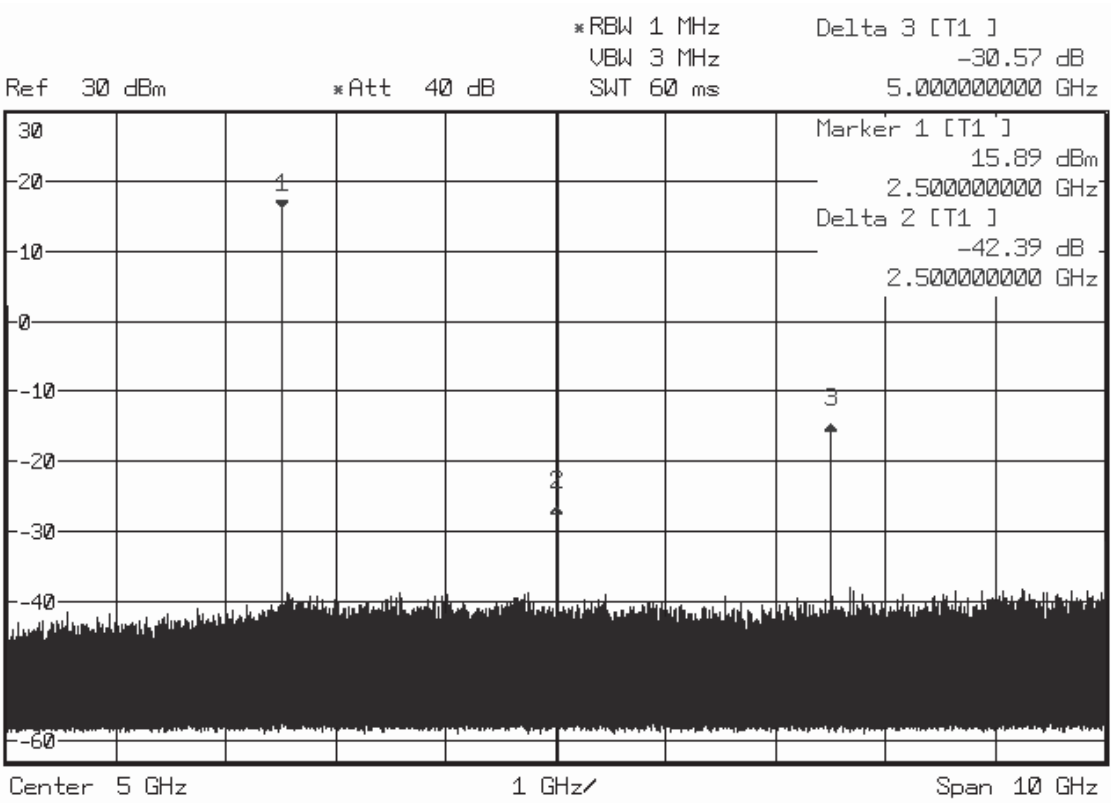


Figure 4.16: Measured spectrum of the class EF2 power amplifier.

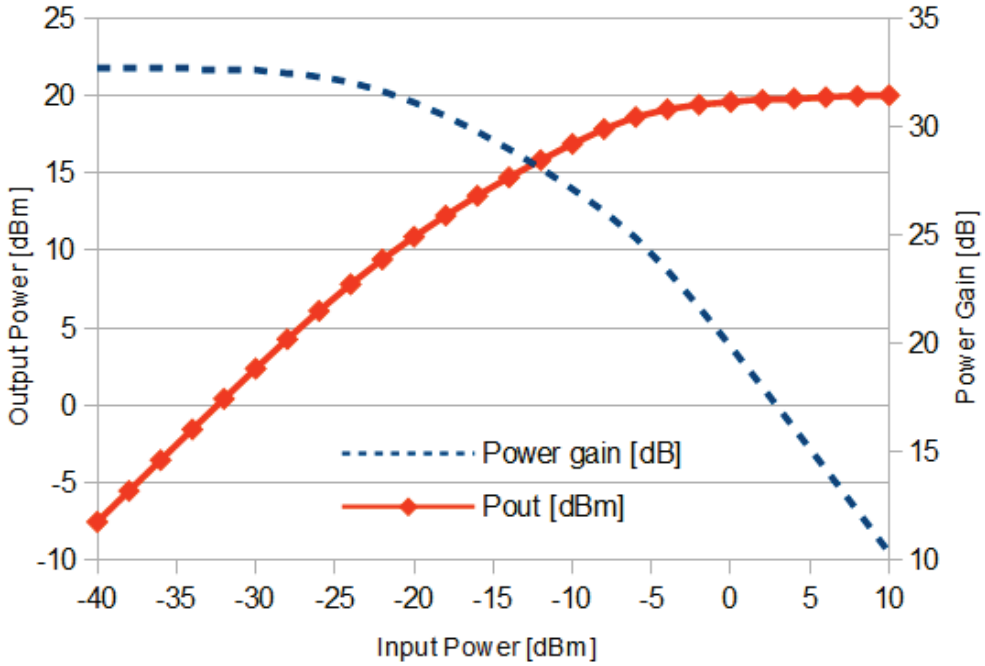


Figure 4.17: Simulated output power and gain versus input power.

degenerating the source of the power device made earlier still hold true for this circuit. As the oscillator generates its own output without the need of an RF power input, the notion of power gain cannot be defined. But in order to understand how the reduction of the gain of the power amplifier can affect the performance

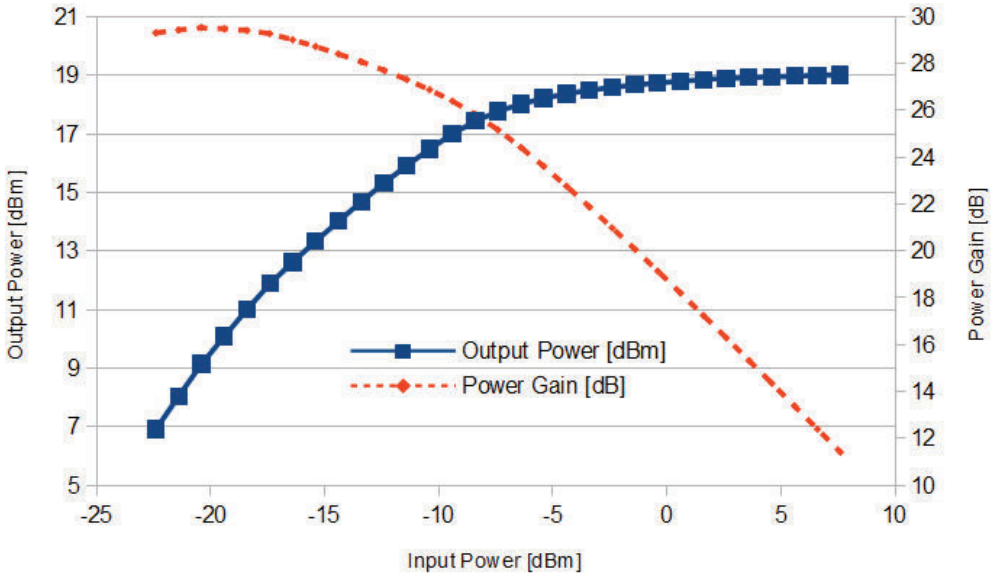


Figure 4.18: Measured output power and gain versus input power.

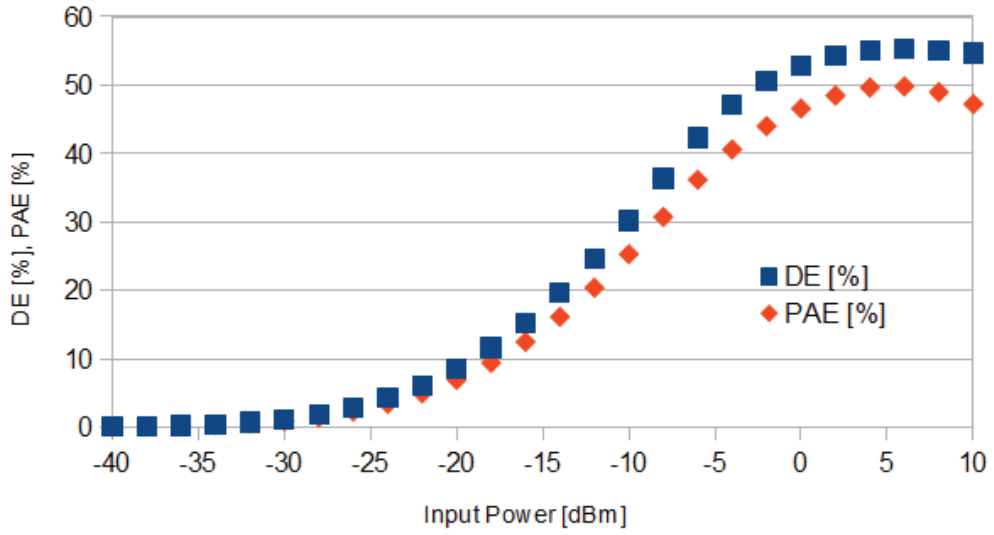


Figure 4.19: Simulated efficiencies: DE and PAE

of the oscillator, a mental experiment can be made.

Suppose one opens the feedback network generating an input port and transforming the oscillator into a power amplifier with an unmatched input. Suppose now an adequate power source capable of driving the input impedance is connected to this power amplifier in a way the output signal is exactly the same generated by the oscillator.

Maintaining the input power constant, if the inductive parasitics degenerate the source of M1, the gain of the power amplifier will be reduced and, consequently, the output power will be reduced. This simple analysis already shows that there is a strong sensitivity of the output power in respect to the source degeneration of the power device. Nevertheless, this analysis hide one important detail: reducing the output power linearly reduces the power available to the feedback network. If lower power is available to drive the

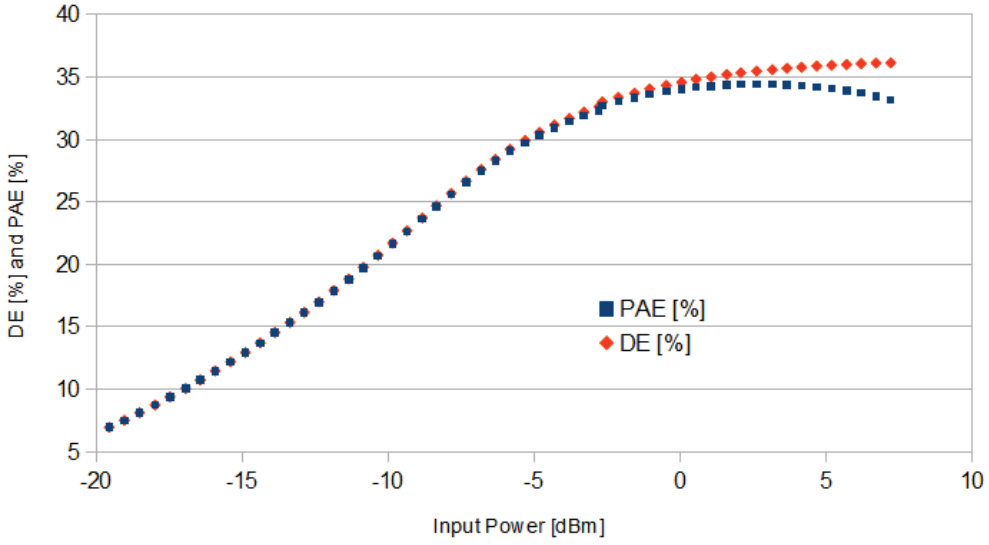


Figure 4.20: Measured efficiencies: DE and PAE

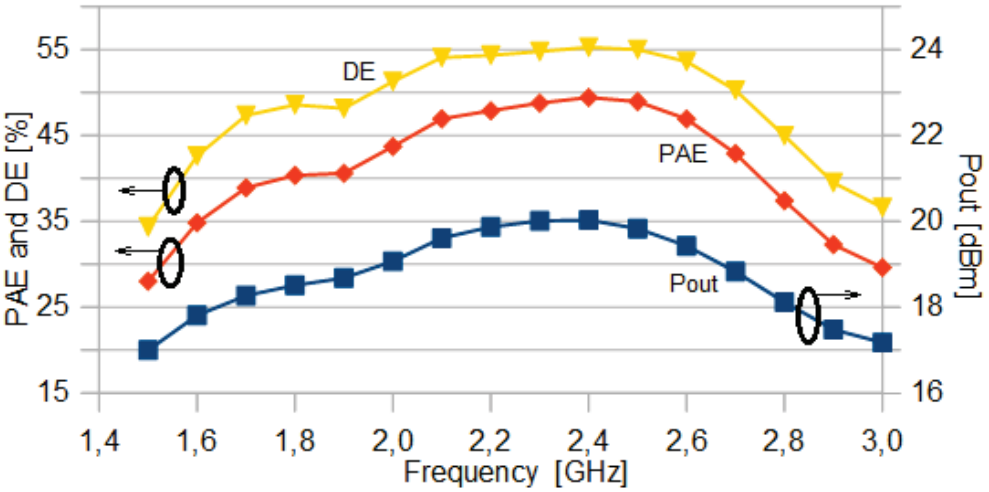


Figure 4.21: Simulated performance over frequency

power amplifier, this will also reduce output power. This leads to the conclusion that inductive parasitics should be minimized at the expense of loosing output power and at the limit, making the circuit not able to sustain oscillation.

In order to address this problem, the same ground plane made for the power amplifier was added in the power oscillator. This should create a large number of parallel paths to ground reducing the parasitics.

A separate supply voltage was used for the driver due to maximum voltage stress M1 transistor may sustain. The drain-bulk parasitic capacitance of M2 is used to implement the capacitance across the switch (C_{SH} in Figure 2.15) and, for that reason, is not present in the schematic. The bias voltage applied to the gate of M2 is used to control the maximum voltage achieved by the drain of M1 and it was chosen to be 2 V in this design, as already discussed. It presents a tradeoff between voltage stress and DC-RF efficiency as a higher value would lead to lower resistance for M2 but would lead to higher stress across M1.

The same analysis made for the power amplifier about the DC biasing, voltage stress on the active

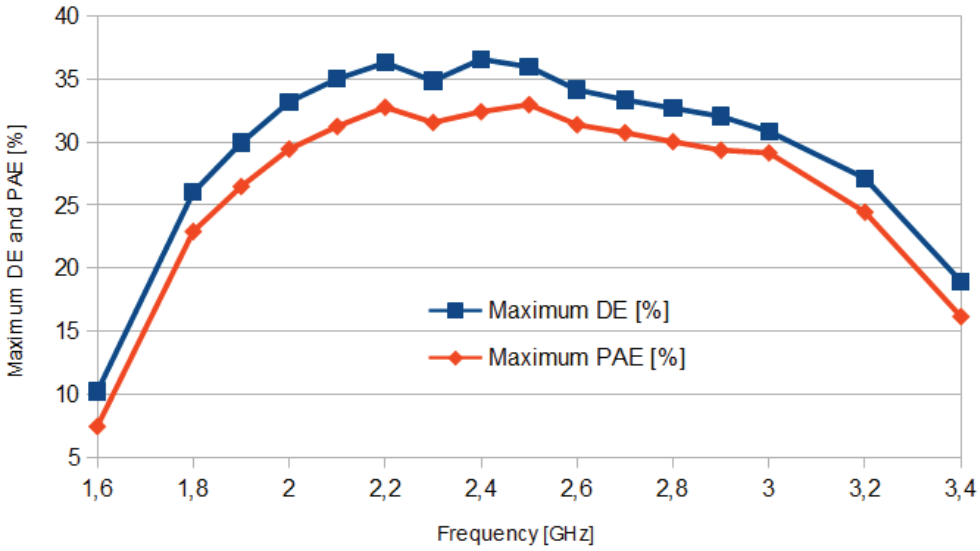


Figure 4.22: Measured efficiencies over frequency

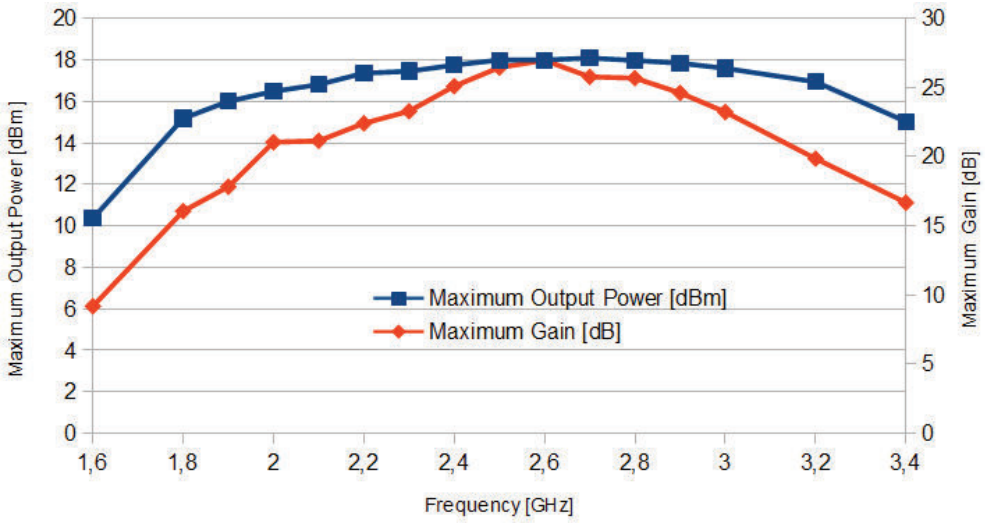


Figure 4.23: Measured output power and gain over frequency

devices, stability issues such as capacitive decoupling of DC voltages and the addition of biasing resistors hold true for the oscillator, as both circuits are very similar.

In the oscillator, the addition of C_n did not have a significant effect on the DC-RF efficiency and for that reason it was not used. The parasitic capacitances have been used in the passive network to implement the waveform engineering.

A first implementation of the oscillator was made using diode varactors due to better linearity of the voltage to frequency transfer function. This approach was changed because, during the positive cycle of the generated RF signal, the diode was taken into conduction compromising the robustness of the gate of the driver stage.

The varactor was finally implemented using MOS transistors connected as varactors. The use of devices modeled to be varactors by STMicroelectronics was not possible because a thick oxide process option was

Table 4.1: Comparison among other PA found in the literature

Work	Class	Frequency [GHz]	Output Power [dBm]	Supply Voltage [V]	PAE [%]	High Voltage Option	Technology
[35]	E	1.8	31.5	3.5	51	yes	CMOS 130 nm
[32]	E	1.7	23	2.5	67	yes	CMOS 130 nm
[40]	E	2.4	9	1.2	30	yes	CMOS 90 nm
[33]	E	2.4	5.7	0.5	55	no	CMOS 130 nm
This work	EF2	2.5	20	2	49.8	no	CMOS 130 nm

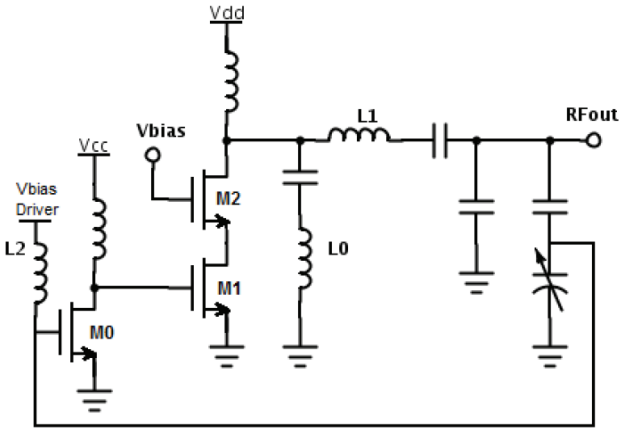


Figure 4.24: Schematic of the implemented power oscillator

needed. As the transistors were not modeled to be used as varactors, some error in the voltage to frequency transfer function may occur.

As well as discussed for the power amplifier, the inductors were taken from a library and designed to present a quality factor higher than 10 around the frequencies of interest. In the case of the inductor marked as L0, the quality factor was optimized to frequencies around 5 GHz as the series LC tank should implement a short circuit around that frequency. Due to the high current that must go through L1, a large metal width was used.

4.3.1 Power Oscillator Simulations and Measurement Results

The micrograph of the prototyped power oscillator is shown in Figure 4.25. The circuit occupied 1550 μm x 1280 μm including pads in standard 130 nm STMicroelectronics technology. This technology provides 1.2 V transistors and 6 metal layers.

Similarly as discussed for the PA, the design of the circuit was made using intensive simulations with the same main goals: RF power and efficiency.The oscillator has other important characteristics that can not be neglected such as phase noise and tuning range.

The simulated current and voltage waveforms are presented in Figure 4.26. As discussed for the PA, a small overlap can be observed and the voltage stress is also kept under tolerable voltage stress limits [32].

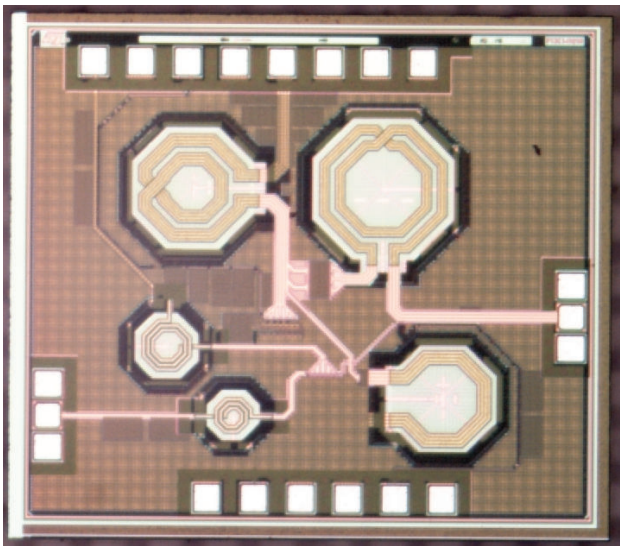


Figure 4.25: Micrograph of the prototyped class EF2 power oscillator

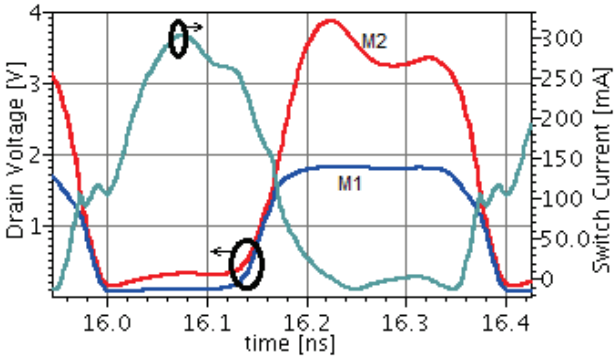


Figure 4.26: Simulated current and voltage waveforms in the class EF2 power oscillator

Once the oscillator generates its own output from a DC supply voltage and this power was made to be large, it is impossible to measure the small signal S parameters. The first measurement used a spectrum analyser to characterize the power spectrum. The expected results are shown in Figure 4.27. It can be noticed the lower power in the 2nd harmonic as it is characteristic in the class of operation. A large difference is found between the fundamental and the 3rd harmonic, which is the strongest of all the harmonics. It can be observed that the circuit should be able to deliver 20 dBm when operating under nominal conditions. These nominal conditions were designed to keep the voltage stress under the limits dictated by the technology.

The measured spectrum under nominal conditions can be seen in Figure 4.28. It can be noticed that the output power has been strongly reduced, around 8 dB. As a consequence of the output power, as commented earlier, the signal at the input of the driver stage is weaker. For this reason, one can notice that the power in the 3rd harmonic is around 10 dB lower than what was expected in simulation. The harmonic generation is a characteristic of the switching-mode power circuits and the lower 3rd harmonic clearly states that the switching is not occurring properly. The 2nd harmonic presents approximately the power it should according to simulation. Supposing the short circuit to this harmonic works as expected, its power

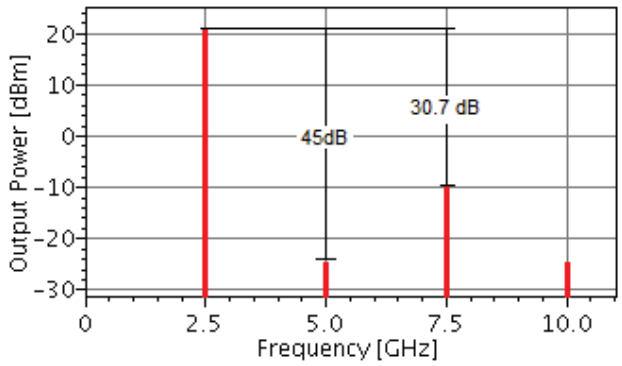


Figure 4.27: Simulated spectrum generated by the power oscillator.

should not increase with the generated power. This hypothesis can be confirmed by increasing the output power by increasing the supply voltage and comparing the power in this spectrum. The result of increasing the supply to 2.5 V is shown in Figure 4.29.

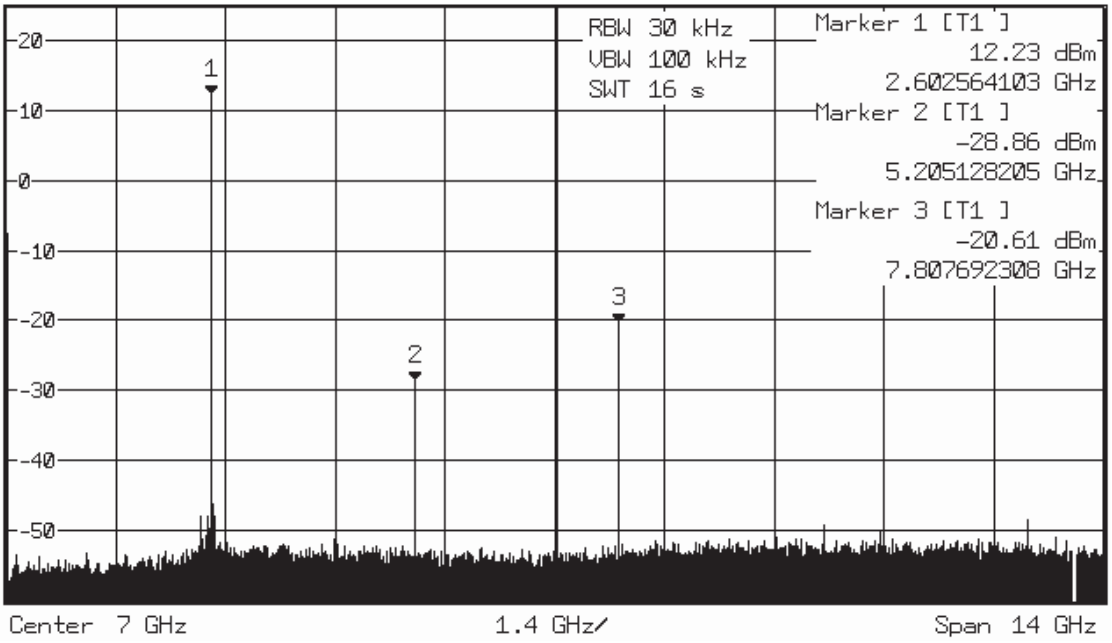


Figure 4.28: Measured spectrum generated by the power oscillator at nominal biasing.

It can be seen that the main difference observed is the power in fundamental and 3rd harmonic. This measurement is closer to the expected result in all ways: fundamental power, power in 2nd and 3rd harmonics and power difference between harmonics. This states that short to the second harmonic works as expected and the circuit is able to deliver the amount of power expected with a change in polarization conditions. The result presented in Figure 4.29 shows that the both switching characteristic and the class EF2 works properly. One possible explanation to this behavior may be the parasitics included by the measurement setup and, as it was concluded for the power amplifier, the design of a PCB could strongly increase the measured performance under nominal conditions. The goal of this PCB should be to decouple the supply voltages as much as possible and provide a low impedance ground path.

It is important to measure the voltage to frequency transfer function as this function will be useful

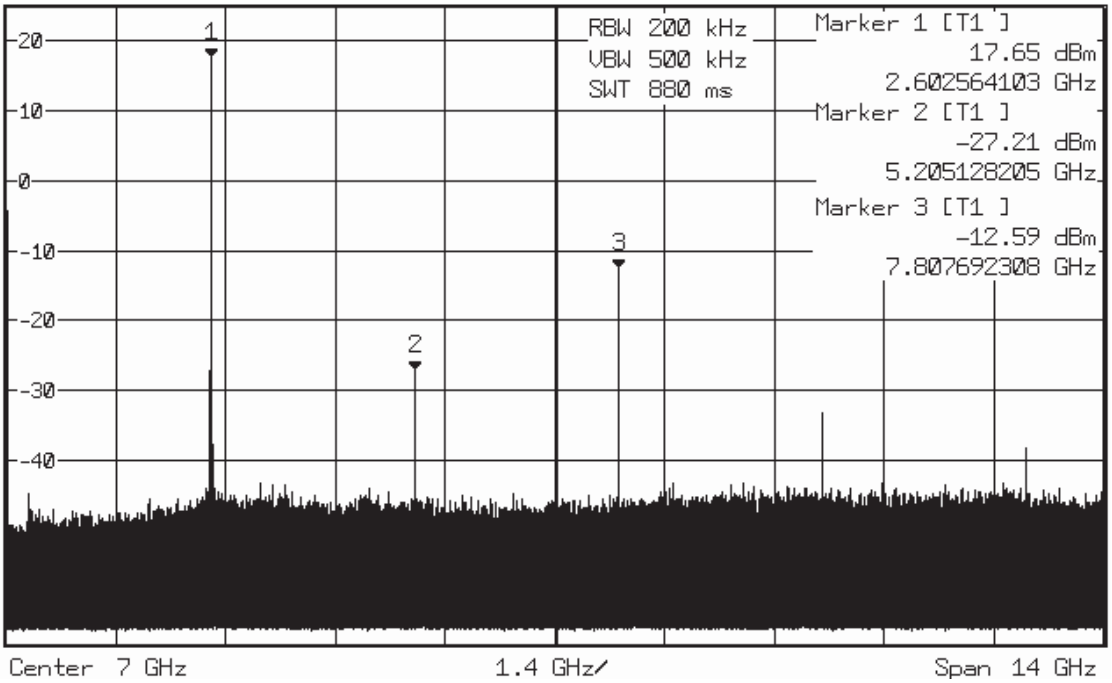


Figure 4.29: Measured spectrum generated by the power oscillator at 2.5 V supply voltage.

for the PLL design. This measurement consists on applying a fixed voltage to the control and measure the fundamental oscillating frequency. The expected voltage to frequency transfer function under nominal biasing conditions is presented in Figure 4.30.

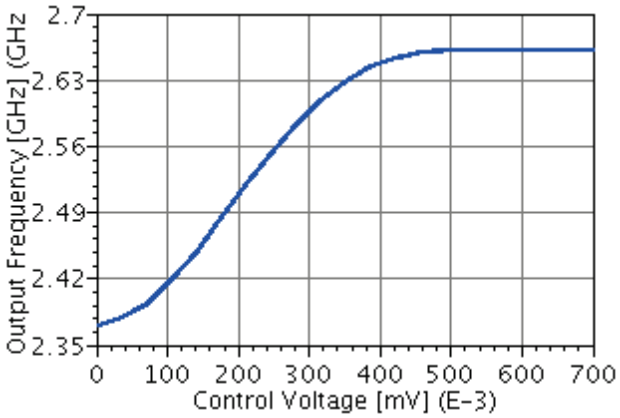


Figure 4.30: Simulated voltage to frequency transfer function.

The non-linear characteristics are given by the use of a MOS varactor. This type of chosen due to a large forward biasing in PN junctions varactors. The measured characteristics are shown in Figure 4.31. A compression of the tuning range can be observed, mainly in the lower frequencies. The compression is found to be around 100 MHz, which is a fairly large value when comparing to the total frequency span. This could be explained by the fact that ordinary transistors were used to implement the varactors once the modeled varactors from the design kit used a layer that could not be used in this design. Another possible source of variation may come from the fact that the varactor's terminals were drain and source of the transistor while the bulk was connected to the ground plane. As current passes the hole ground plane

develops a potential different from zero due to cabling and ground plane resistances. This bulk-source voltage alters the transistor's capacitance characteristic, changing the oscillating frequency. As the control voltage increases, the transistor becomes inverted and this variation becomes negligible.

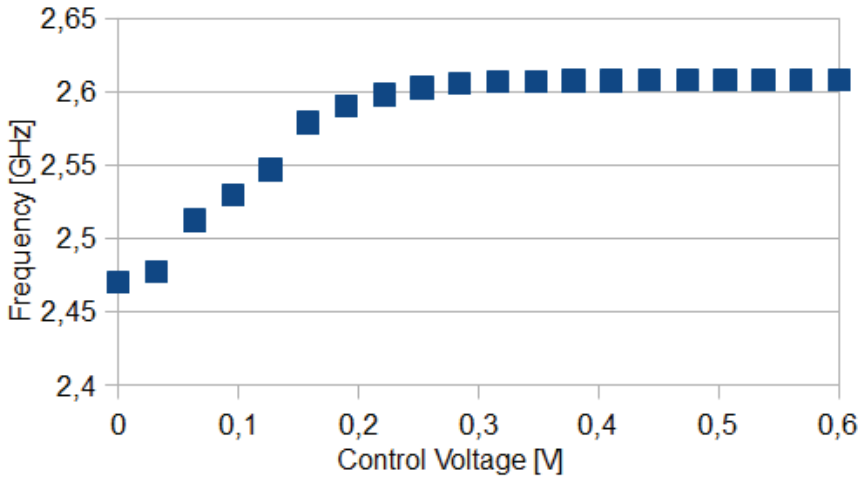


Figure 4.31: Measured voltage to frequency transfer function.

As changing the capacitance of the varactor alters the impedance seen by the load, one can expect a variation in the S22 and, consequently, a mismatch between the oscillator and the load. This will be reflected in a dependence between output power and the control voltage. This dependence should be minimized in the design and this can be accomplished by using a large bandwidth power amplifier with a large bandwidth impedance matching. The simulated characteristic for the generated power as a function of the control voltage is shown in Figure 4.32.

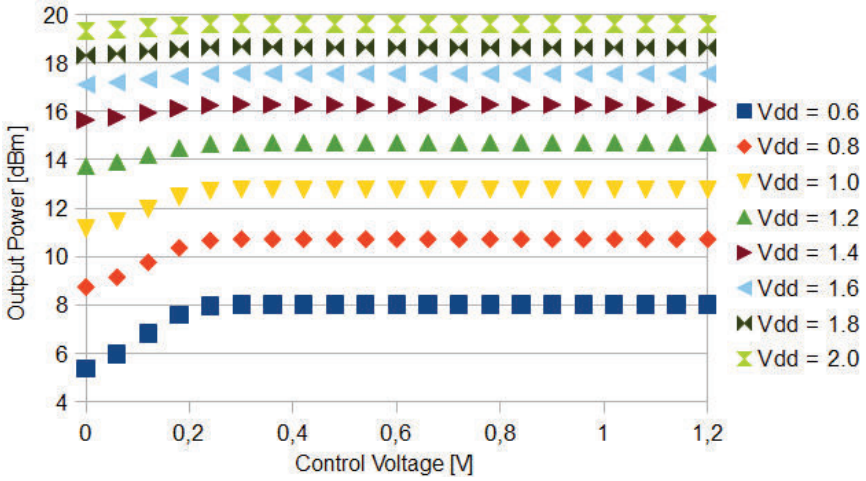


Figure 4.32: Simulated dependence between output power and control voltage.

It can be seen that for higher values of supply voltage, and consequently higher power levels, the power variations become less noticeable. This can be explained by the variation of the matching conditions caused by large signal variations. The circuit was designed to behave as well as possible with larger output power. In nominal conditions (vdd = 2 V), the output power varies 0.24 dB along all tuning range.

The measured characteristics are shown in Figure 4.33 for supplies from 1.6 V up to 3 V. Qualitatively,

it is observed the same behavior in which the input power grows with the control voltage. Nevertheless, the curves are not well behaved and do not show a steady trend, mainly for lower supply voltages. The most well behaved curve is the nominal operation condition. In this curve, a power reduction of almost 3 dB can be observed as well as a degradation in the power immunity to frequency variation.

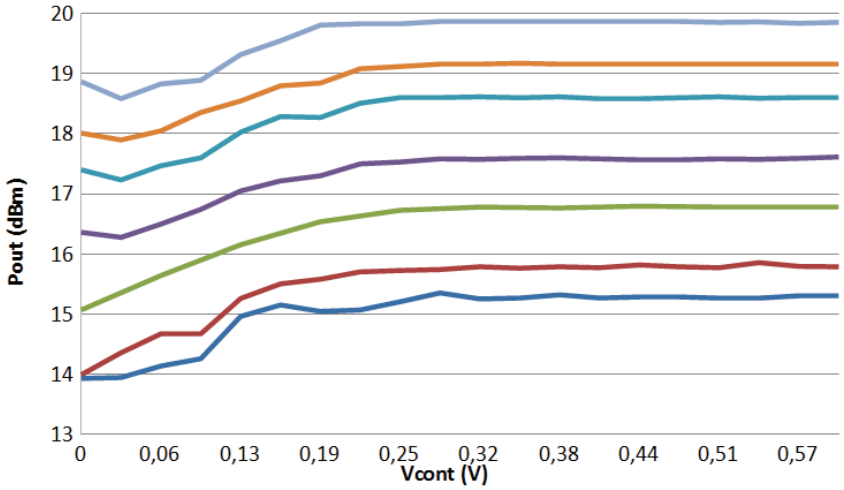


Figure 4.33: Measured dependence between output power and control voltage.

Despite the reduction in RF power that has been observed in both the power amplifier and the power oscillator, the switching characteristics of the circuits can be verified. In circuits such as these, the output power is ideally dependent with the square of the supply voltage. Once the power is measured in dBm, a straight line should be obtained as it can be seen in Figure 4.34. This characteristic is very important once it makes possible, and relatively easy, the amplitude modulation of the generated signal. This result shows that the power stage is actually switching as it would be expected. This result also reduces any doubts on the correct operation of the circuit.

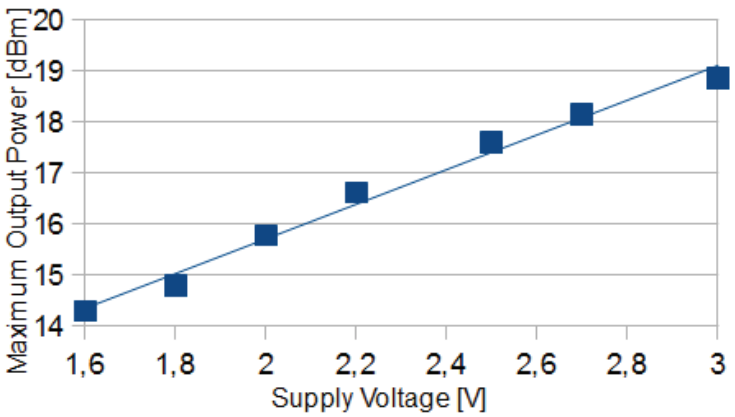


Figure 4.34: Measured transfer function from supply voltage to output power.

One important aspect is to observe how the harmonics behave along the tuning range. As needed for class EF2 correct operation, a short circuit to the second harmonic must be made across the switch. The existence of this short for all possible generated frequencies makes possible the use of the lower voltage stress along all the tuning range. A problem in this harmonic can jeopardize the active devices lifetime

once the voltage stress would be larger for the same output power. The simulated power in each harmonic in nominal biasing conditions along the tuning range is shown in Figure 4.35.

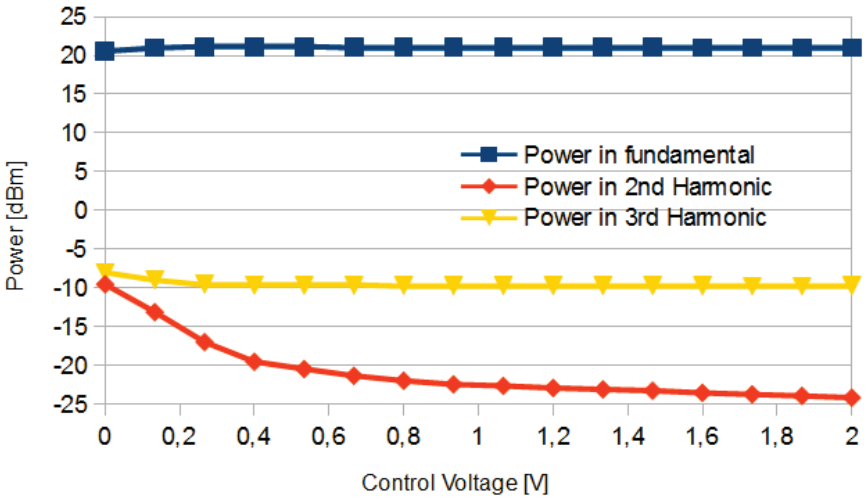


Figure 4.35: Simulated power in each harmonic along control voltage.

It can be seen that the power in 2nd harmonic is always lower than the power in 3rd harmonic and this ensures correct operation.

In measurement, the same characteristic of lower power in 2nd harmonic hold true for the 3 data samples available and it can be seen in Figures 4.28 and 4.29. This means that the correct EF2 operation is guaranteed in measurement.

The expected DC-RF efficiency of the circuit is shown in Figure 4.36. It can be seen that an efficiency around 40% was expected under nominal biasing conditions and using a 50 Ω load.

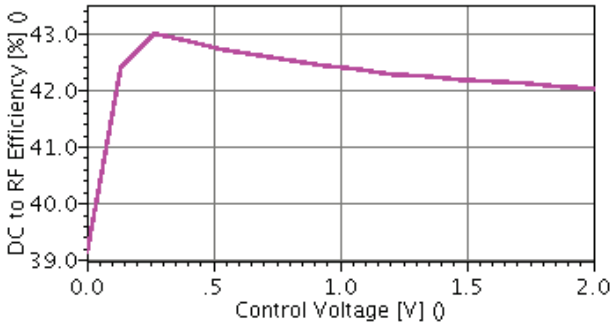


Figure 4.36: Simulated DC-RF efficiency.

In order to measure the efficiency, the load pull setup was used. The result from this measurement is shown in Figure 4.37. It is possible to observe that the impedance for maximum efficiency has shifted away from 50 Ω but the efficiency does not vary much from the optimum to 50 Ω. This emphasizes the large bandwidth of the matching.

The efficiency is seriously affected once the generated RF power has been reduced. Under nominal biasing conditions, the maximum DC-RF efficiency is measured to be 26.82%.

Phase noise is an important characteristic of any oscillator and since the generated signal is intended

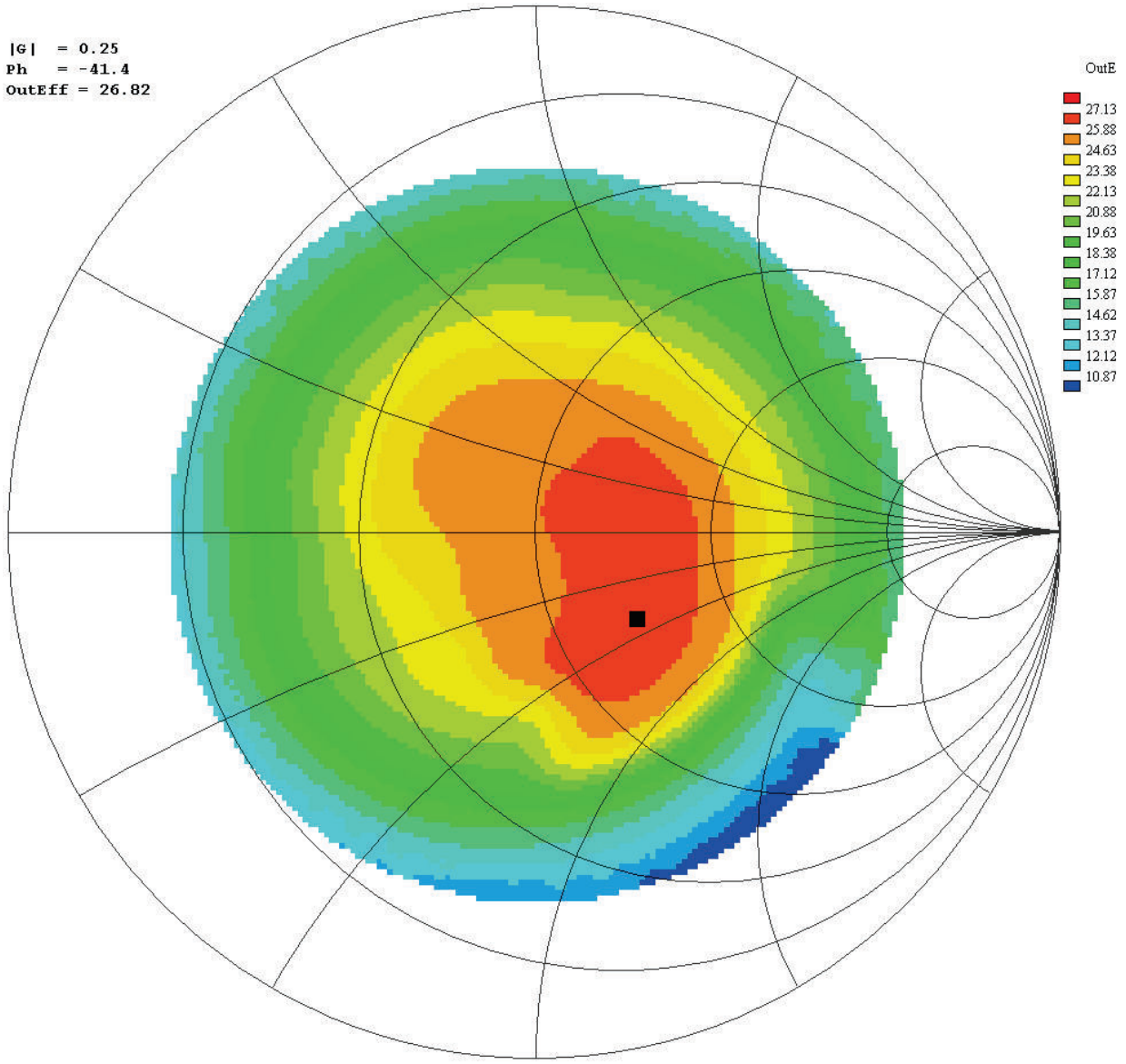


Figure 4.37: Load pull measurement.

to be used directly to carry information, it should be a stable signal. Simulations shown a phase noise as low as -118.8 dBc/Hz at 1 MHz offset such as shown in Figure 4.38. In this Figure it is easy to observe the $1/f^2$ and $1/f$ noise as expected in theory.

The results of the phase noise measurements are shown in Figure 4.39. It can be seen that the noise not well behaved and the measurements are not well reproducible indicating that the setup may be limiting the performance. As DC noise gets up-converted by the switching operation of the circuit, a more stable supply should be provided. The measurements show a 17.2 dB difference in the phase noise. Further improvement in the setup are needed to address the 17 dB noise difference, misbehavior in the curves and irreproducibility.

As introduced in [74], the following figures of merit are used in this work:

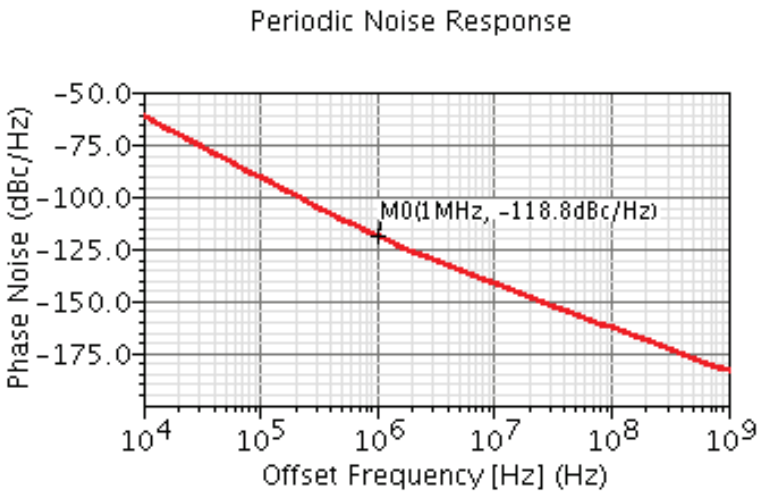


Figure 4.38: Simulated phase noise.

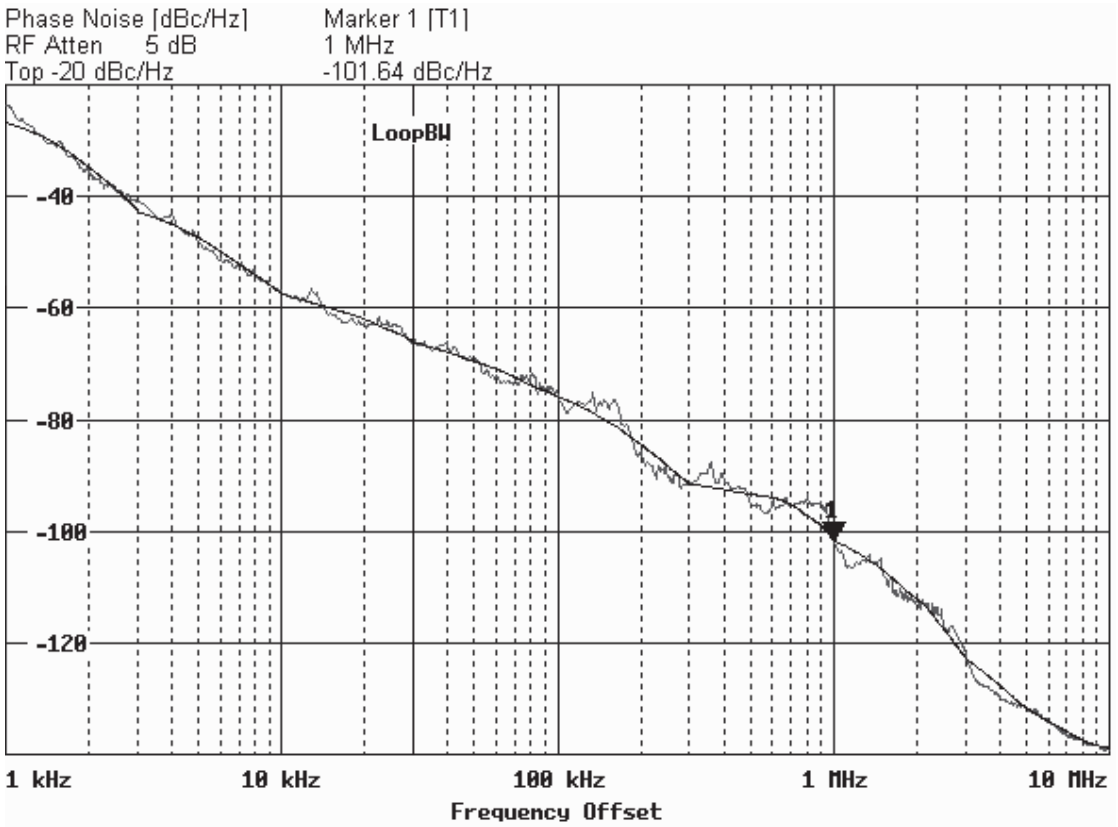


Figure 4.39: Measured phase noise.

$$FOM_p = \mathcal{L}\{\Delta f_{offset}\} - 20 \cdot log\left(\frac{f_0}{f_{offset}}\right) - 10 \cdot log\,\eta \tag{4.11}$$

$$FOM_{POSC} = FOM_p - 10 \cdot log\left(\frac{P_{RF}}{1mW}\right) \tag{4.12}$$

Table 4.2: Comparison among power oscillator from the literature.

Work	Frequency [GHz] [GHz]	Output Power [dBm]	Vdd [V]	Tuning Range [MHz]	DC-RF Efficiency [%]	Technology	FOM_p	FOM_{POSC}
[50]	2.4	27	6	80	42.5	PHEMT	-182	-209
[49]	0.9	8.5	1.2	-	46.5	PCB	-	-
[4]	1.95	23.3	2.5	400	60.3	CMOS 65 nm	- -	- -
This work	2.5	20.6	2	300	42	CMOS 130 nm	-183 -	-196.1 -

Equation 4.11 takes into consideration parameters from ordinary oscillators, i.e. not designed to deliver high power, such as phase noise ($\mathcal{L}\{\Delta f_{offset}\}$) at a given frequency offset f_{offset} and other parameters from high power circuits such as DC-RF efficiency η. On the other hand, Equation 4.12, take into consideration the generated RF output power.

For the sake of comparison among other works, Table 4.2 present other power oscillators in RF frequency. Notice this type of circuit is rarely published and often parameters such as phase noise is not informed. It can be seen that the presented power oscillator delivers comparable amount of RF power using a standard CMOS technology without high voltage devices. It can also be noticed that phase noise information is often not given and this is the reason the FOMs could not be calculated for every circuit. When comparing FOMp between [50] and this work, it can be seen that both works are very similar. In FOMposc, the circuit presented in [50] takes the lead due to the higher output power. It must be noticed, though, that the technology used is capable of dealing with much larger voltage stresses than standard CMOS.

The results presented in [4] and this work are post-layout simulations.

4.4 HIGH LEVEL MODELING OF THE POWER OSCILLATOR

The analysis of modulated signals demand simulation of several symbols. As the symbol rate is often orders of magnitude lower than carrier frequency, the simulation of complete communication systems is hard, and often impossible, to be done in transistor level. One approach for simulating systems is the creation of high level models that describe the behavior of each circuit and use these simplified models to evaluate the performance of the system.

In the case of the RF transmitter based on the power oscillator this exact problem is faced. The symbol rate is in the order of magnitude of hundreds of kbps while the carrier frequency operates at 2.5 GHz. In order to obtain numeric convergence, transient simulation calculate points at time steps that are much smaller than carrier period, around some hundreds of picoseconds. Hence, the simulation of an amount of time enough for evaluating tens of symbols is very large due to the enormous amount of simulated samples.

Another possibility is to use envelope simulations. This simulation simulate the circuit in a mixed time-frequency domain and it is able to abstract the carrier frequency, using larger time steps, comparable with the symbol period.

The simulator provided by Cadence is used for these simulations and envelope simulation is no able to deal with high level models. Reasons for the use of these models are discussed in Section 4.5. Therefore, the only option left for simulating the complete system is ordinary transient simulation.

A high level model of the oscillator was developed using post-layout simulations and can be easily altered to reflect the measured characteristics. The goal with this model is to reduce the amount of calculations needed, reducing the simulation time. Instead of solving the circuits equations on each time step as the schematic or extracted view would demand, the model uses a table to describe the behavior of the circuit.

The model was based on a table of simulated values and the functions "$table_model" available in veriloga language. This function must receive a file containing a lookup table and interpolation method desired. Due to a large number of points, linear interpolation was used.

The two most important characteristics of the oscillator were modeled: (i) voltage to frequency transfer function and (ii) supply modulation transfer function. The results obtained are the same as presented in Figures 4.30 and 4.32.

4.5 RF TRANSMITTER ARCHITECTURE

Using the know-how obtained so far, it is possible to propose a transmitter architecture that uses a power oscillator to generate modulated signals. This architecture will be very similar to the one presented in Figure 4.2, based on a PLL.

When simulating an up-conversion RF system, the simulator must deal with radically different frequencies: (i) the carrier, in this case around 2.5 GHz, and (ii) the data rate, up to some MBps. As one is interested in observing how the system works, long simulations, able to cover many different symbols, must be run. With the need for long simulation time, computational effort becomes an issue and ways to decrease simulation time become essential for the design to be feasible.

Answering to this problem, a verilogA model of the whole transmitter was made. Beside the model of the power oscillator, cells from Cadence ahdlLib, analogLib and pllLib were used. Using verilogA avoids the need for complex transistor level models of each circuit and can speed up the simulation time. It is important to mention that the high level simulation will be accurate if the models take enough behavior in account. This trade off between simulation time and accuracy has been treated in [75] and [3] and is beyond the scope of this text.

The created system is depicted in Figure 4.40. In order to demonstrate the feasibility of the solution, the AM loop is kept open. For the power oscillator under analysis, AM modulation can be obtained with reasonable linearity observing Figure 4.34. In this way the system was simplified, without loss of generality.

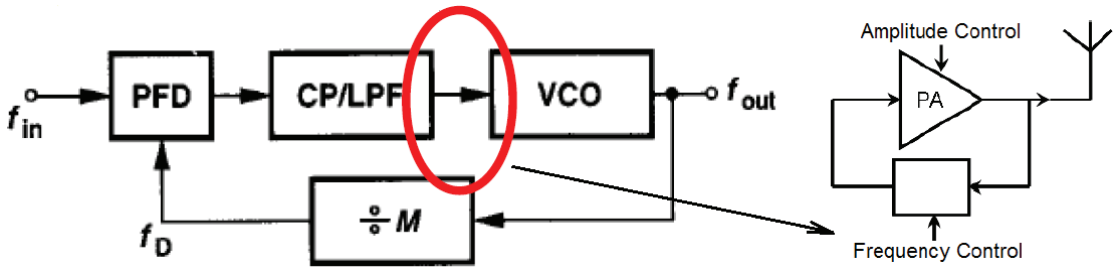


Figure 4.40: Simulated RF transmitter based on a power oscillator.

Knowing that any modulated signal can be written as shown in Equation 4.13:

$$s(t) = A(t) \cdot sin(2\pi ft + \Phi(t)) \tag{4.13}$$

where $A(t)$ is the amplitude modulation and $\Phi(t)$ represents the angle modulation, it is possible to treat modulation and phase modulations separately.

To maintain compatibility with Section 4.1, the discussion starts by amplitude modulation. In this case, the PLL was set to work at a constant frequency and the supply voltage of the power oscillator was modulated with a sine wave. It is important to remember that the DC level of the supply voltage controls the output power level. This variable is kept constant for this simulation.

4.5.1 PLL Lock Acquisition

First of all, it is important to show the PLL is able to acquire lock with no modulation. A simulation in which the reference frequency is set to 24 MHz and the divide ratio to 104, leading, ideally, to an output frequency of 2.496 GHz is shown in Figure 4.41. In this simulation, the supply voltage is kept at 2 V leading to 19.5 dBm ($3V_{peak}$ over a 50 Ω load). The curve on the top shows the voltage on the load resistor (net /out). The second curve depicts the control voltage (net /vcont) and the instataneous frequency of the output voltage. The third curves are inputs of the PFD. The curves at the bottom of Figure 4.41 present the outputs of the PDF responsible for increase and decrease in output frequency.

The vertical cursor shows the obtained values:

- $2.99V_{peak}$ on the 50 Ω load;
- Observing the control voltage locked at 187.65 mV;
- The loop locked at 2.496 GHz as expected;
- Both control signal (up and down) are zero after a stabilization time.

It is interesting to mention that the PLL linearizes any phase non-linearity of the power amplifier leading to a highly linear device.

4.5.2 Amplitude Modulation

To demonstrate the amplitude modulation capability, the supply voltage of the power oscillator was changed to $1.9V_{DC}$ and a sinusoidal signal of $300mV_{peak}$ with 50 kHz was added. The result of a transient simulation is shown in Figure 4.42. The curve on the top shows the voltage on the load resistor (net /out). The second curve depicts the control voltage (net /vcont) and the instantaneous frequency of the output voltage. The third curves of Figure 4.42 present the outputs of the PDF responsible for increase and decrease in output frequency. It is possible to observe that they are not always at zero voltage and feedback is constantly active. The curve at the bottom is the supply voltage of the power oscillator.

It is possible to observe that the output voltage on the load resistor follows the supply voltage as expected, generating a change in the output power. This demonstrates the capability for AM modulation. Although the problems of phase and amplitude modulation are treated separately in this text, for clarity sake, it is observed that this is not true for the case of AM modulation. Supply modulation alters the parasitic capacitance of the transistors which adds a parasitic frequency shift in the power oscillator. This frequency shift is corrected by the loop and correct amplitude modulation is obtained. The AM modulation then becomes also limited by the bandwidth of the PLL since the frequency must be corrected as the modulation is made.

4.5.3 Frequency and Phase Modulation

The problem of modulating the frequency and phase of the proposed transmitter is now investigated. Beginning the study by frequency modulation, the supply voltage of the power oscillator is kept constant at 2 V. Frequency modulation is obtained by altering the division ratio of the PLL. Maintaining the frequency reference at 24 MHz and altering the digital divider between 104 and 104.5, output frequencies of 2.496 GHz and 2.508 GHz should be obtained. This demonstrates a 2FSK modulation.

The result of a transient simulation is shown in Figure 4.43. The curve on the top shows the voltage on the load resistor (net /out). The second curve depicts the outputs of the PDF responsible for increase and decrease in output frequency. The third curve of Figure 4.42 presents the control voltage (net /vcont) and the instantaneous frequency of the output voltage. As it can be observed, the transmitter works as supposed.

The spectrum generated by the transmitter for the 2FSK signal is shown in Figure 4.44. It can be noticed that the peaks occur at the desired frequencies. Much energy leakage is observed in this Figure due to DFT algorithm and not optimal sampling due to computational effort.

Now, instead of modulating frequency, phase modulation will be treated. Using the same modeled hardware, a BPSK signal around 24 MHz is presented at the reference. A BPSK signal is used for its simplicity and because it provides the worst case in phase shift, i.e. 180°. In this simulation, the supply voltage of the power oscillator is still kept at 2 V for high power generation.

The transient simulation for the BPSK signal is shown in Figure 4.45. The curve on the top shows the control voltage (net /vcont). The third curves are inputs of the PFD, the input modulated reference and the fedback signal. The curves at the bottom of Figure 4.45 present the outputs of the PDF responsible for

increase and decrease in output frequency.

It is possible to observe that the reference switches 180° at 52.5 μs. The PLL then reacts locking the output phase with the altered reference, as expected. A detailed picture around the switching moment is shown in Figure 4.46.

Usually, digital data is shown using constellations. This kind of presentation demands the so called Envelope Simulation. It is more computationally efficient than ordinary transient simulation as it is able to simulate the circuit in the domain of the envelope. This simulation algorithm avoids the very different frequencies by using harmonic balance algorithm continuously over time.

The Envelope Simulation demands the circuit to be modeled in a complex domain, so it is able to simulate "ïn phase" and "quadrature" signal components. On the other hand, ultimately being an oscillator, the power oscillator model does not provide "ïn phase" and "quadrature" components and for this reason it is not compatible with Envelope Simulation.

In order to work around this issue, different simulators have been used: Spectre and Ultrasim, from Cadence Framework, and ADS. None of them is able to work with verilogA models. Not only the power oscillator but also the other building components. For this reason, constellations are not shown. This poses a serious limitation in the simulation of the system as key parameters, such as EVM and ACPR, are hard to be evaluated.

Notice that absolutely no hardware change was made in order to obtain AM, PM or FM modulations. Only the inputs of the circuit were changed. This proves the architecture to be feasible and very flexible and reconfigurable. Supposing a processor is able to control both amplitude and phase inputs, the RF hardware is able to respond to different situations, modulations and bit rates and power levels.

Mathematics, theory and simulations discourage the use of this architecture in high throughput communication. On the other hand, other applications such as RFID readers and wireless sensor networks, are perfectly suitable and could take advantage of the flexibility demonstrated here.

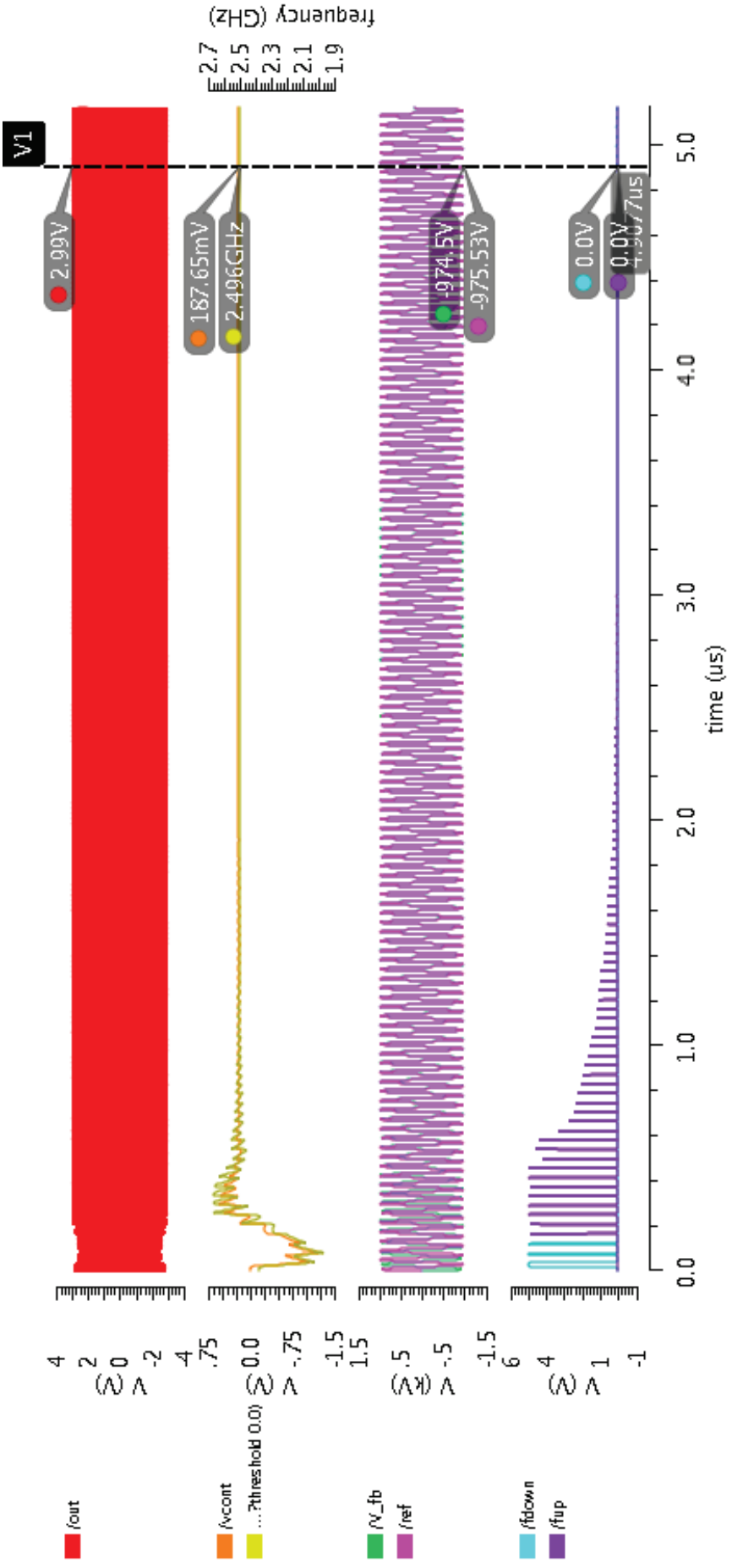


Figure 4.41: Simulation of the PLL using the power oscillator.

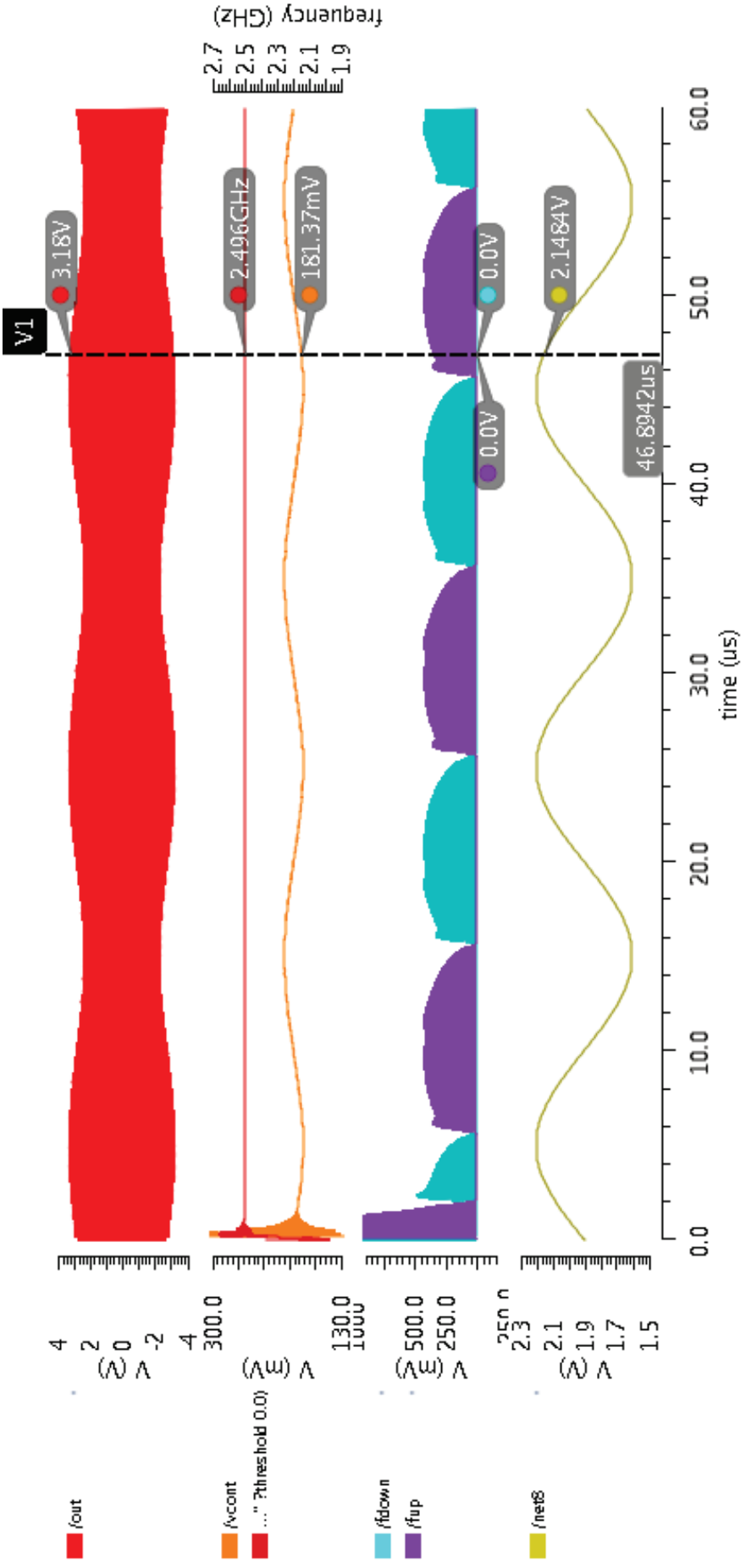


Figure 4.42: Simulation of AM modulation using the power oscillator.

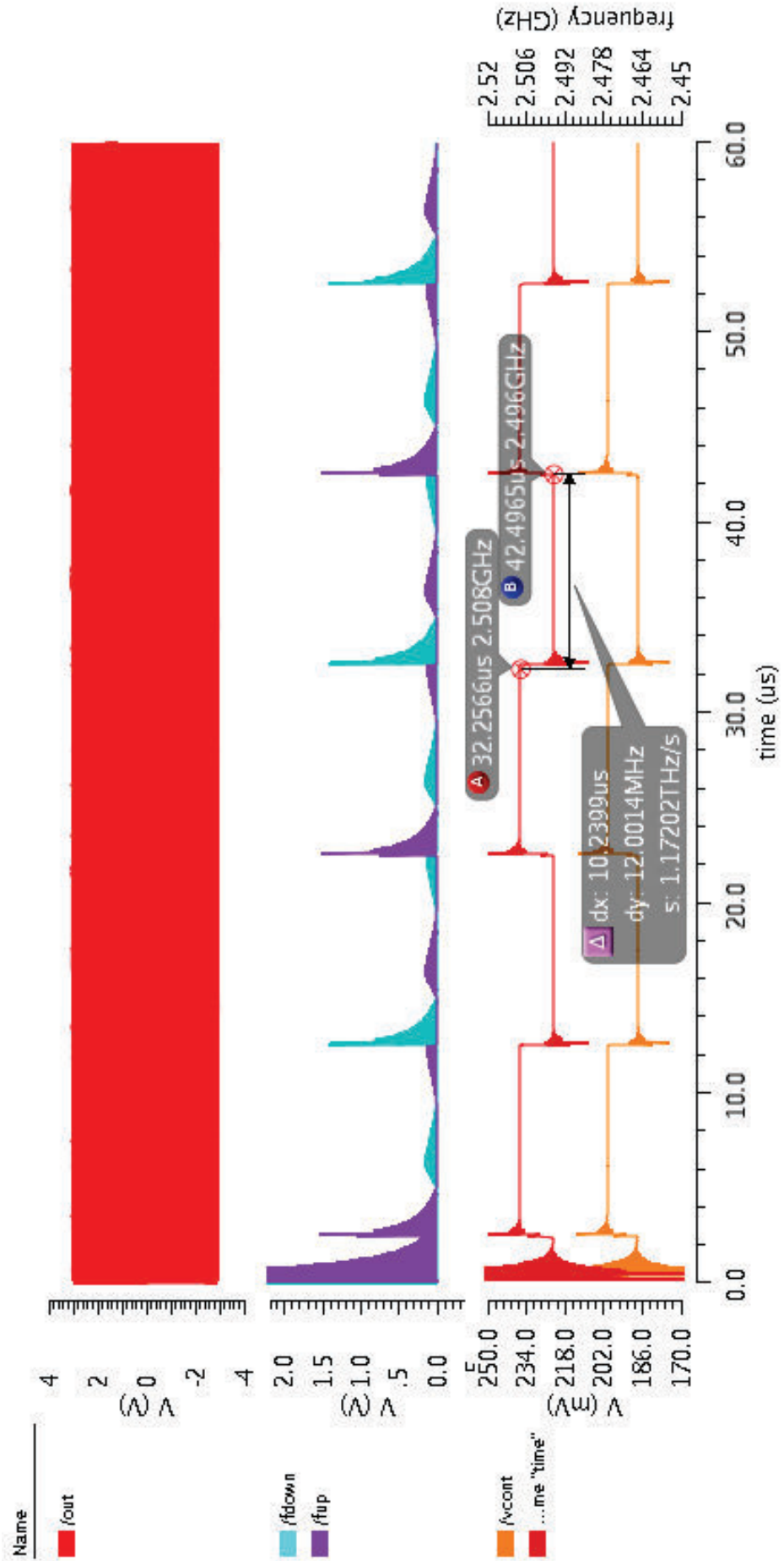


Figure 4.43: Simulation of FM modulation using the power oscillator.

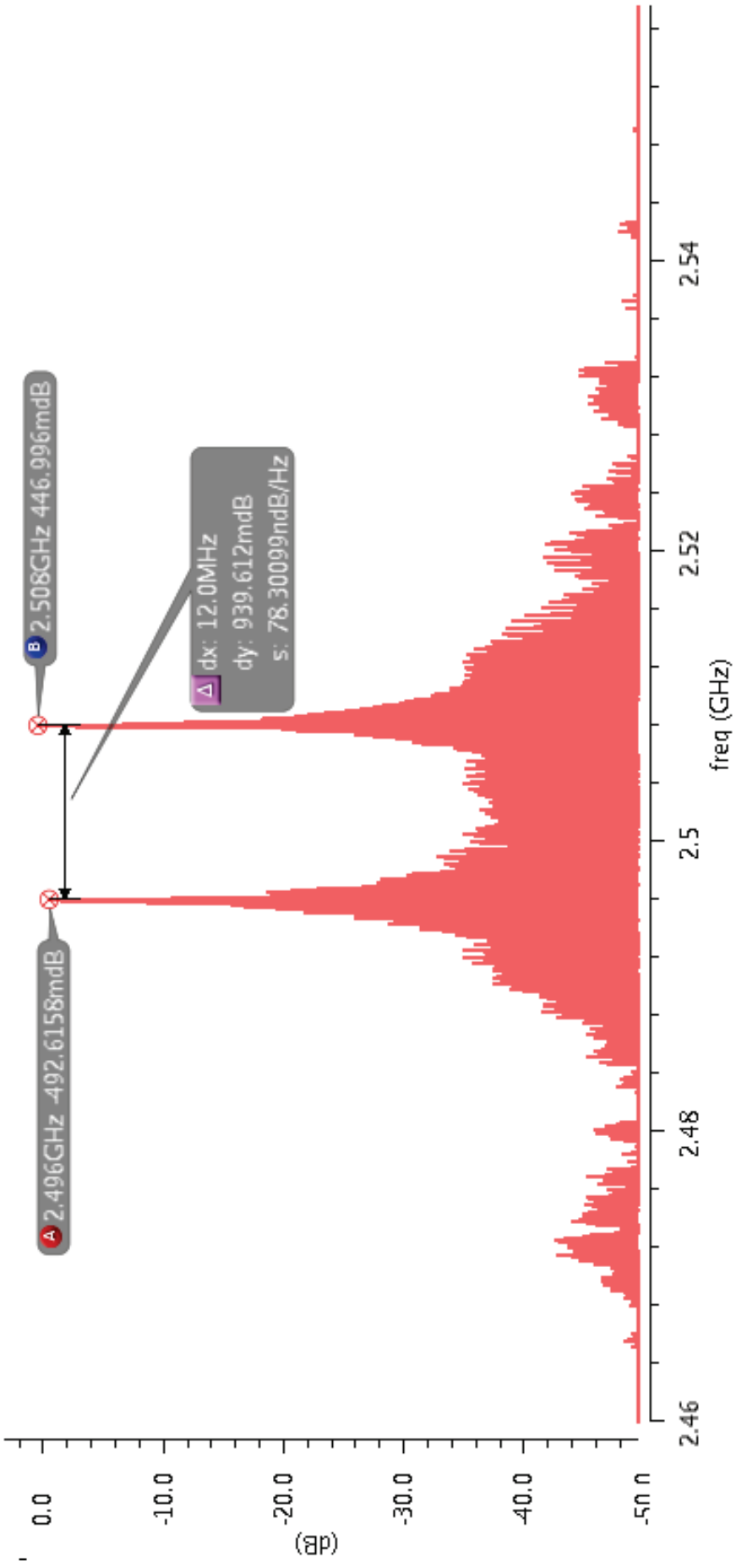


Figure 4.44: Spectrum of the FM modulation using the power oscillator.

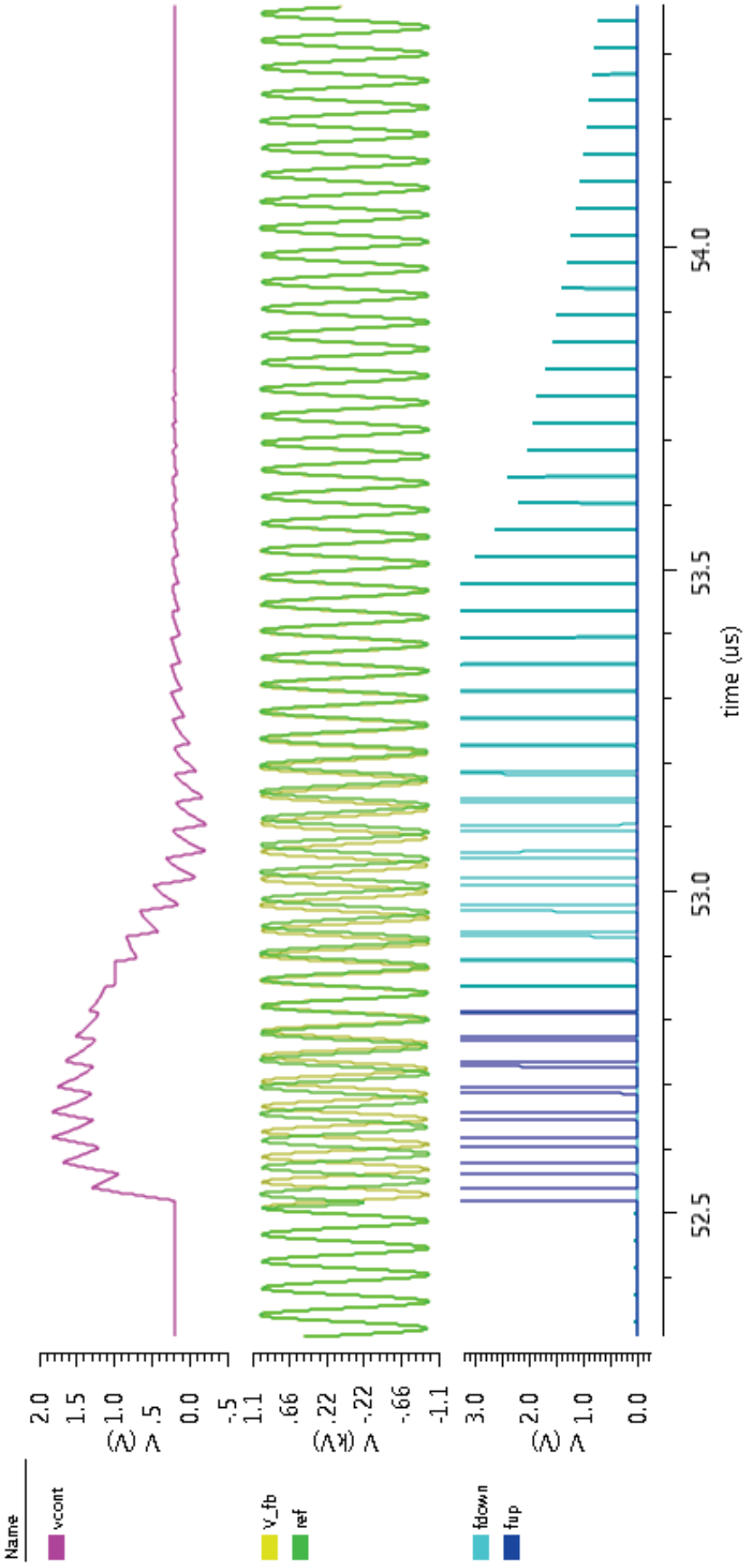


Figure 4.45: Simulation of the BPSK signal using the power oscillator.

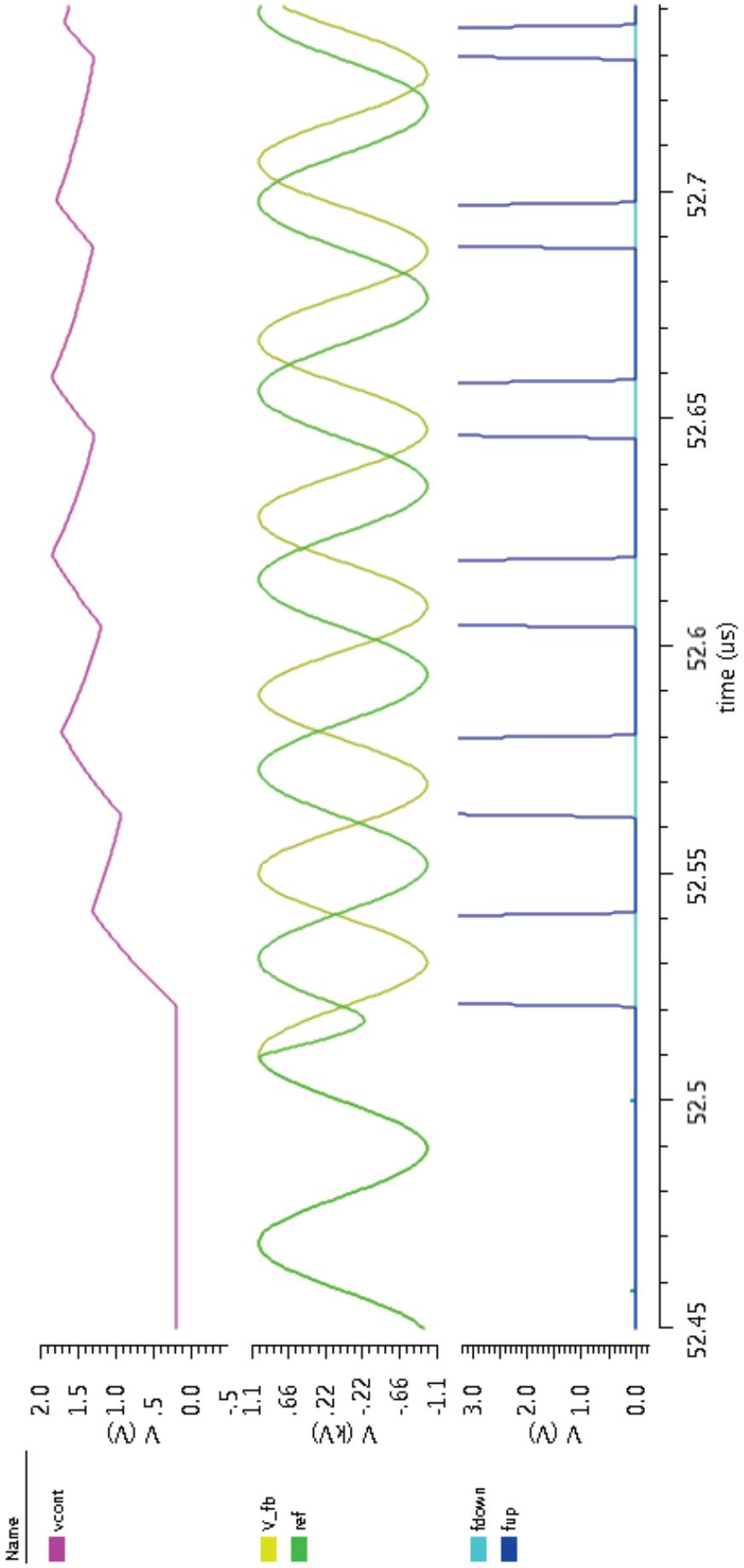


Figure 4.46: Detail of the simulation showing the switching moment.

5 CONCLUSION

The needs for flexible and efficient RF communication led to a complete rethinking of the transmitter. The generation of powerful RF signal using a power oscillator and its modulation allows a complete change in the classical heterodyne and homodyne architectures.

This work presented the design and measurements of a power oscillator that will be used for communication applications. The design used Cadence Framework and standard 130nm CMOS technology from STMicroelectronics. The measurements were carried out in Bordeaux using probe stations giving good signs of correct functionality.

Beside the power oscillator, a power amplifier was designed and measured. As both circuits are internally very similar, this circuit has the goal to give a complete understanding of the RF circuit that is used. Due to the relative low breakdown voltage of the used devices, a solution to generate more RF power with less voltage stress was investigated. The result is the use of class EF2, presented for the first time at RF frequencies.

Both measurements demand improvements and special PCBs are currently under design. These PCB have two main goals: (i) provide more stable DC voltages to the circuit and (ii) reduce the parasitics included by cabling and connectors.

From a system perspective, the feasibility of the use of a power oscillator in an RF transmitter is shown by means of a high level simulation in ADS and a verilogA model built based on the transfer functions of the designed power oscillator. The transmitter is based on a type III PLL and is shown to be flexible and reconfigurable. The same hardware is shown to be able to generate different kinds of modulation such as AM, FSK and BPSK, only altering the input signals. Reconfiguration of output power is also shown to be possible.

A discussion on the limitations of the architecture are made and some mathematical modeling is presented.

Future work includes the complete measurement of the power amplifier and power oscillator using a PCB, the design of the solution in silicon and its measurement.

5.1 LIST OF PUBLICATIONS

During the duration of the research the following papers have been published:

1. Neves, L.C.; de Araujo, G.M.; da Costa, J.C.; Madureira, H.M.G.; Haddad, S.A.P., “UWB pulses generator filter for M-ary communication systems,” 2012 IEEE International Conference on Ultra-Wideband (ICUWB), pp.453,456, 17-20 Sept. 2012

2. Madureira, H.; Deltimple, N.; Kerherve, E.; Haddad, S., “Design of a class EF2 power oscillator for

RF communication application," Electronics, 2013 IEEE 20th International Conference on Circuits, and Systems (ICECS),pp.763,766, 8-11 Dec. 2013

3. Madureira, H.; Deltimple, N.; Haddad, S.; Belot, D.; Kerherve, E., "Design of a Wideband 1.5GHz to 3GHz Class EF2 Power Amplifier", 12th IEEE International New Circuits and Systems Conference (NEWCAS 2014), Jun. 2014

4. Madureira, H.; Deltimple, N.; Kerherve, E.; Dematos, M.; Haddad, S., "Design and measurement of class EF2 power oscillator," Electronics Letters , vol.51, no.10, pp.744,745, 5 14 2015

One final journal paper presenting the results on the transmitter architecture is under final internal revision to be submitted to IEEE Transactions on Circuits and Systems (IEEE TCAS).

REFERENCES

[1] POLASTRE, J.; SZEWCZYK, R.; CULLER, D. Telos: Enabling ultra-low power wireless research. In: IEEE. *Fourth International Symposium on Information Processing in Sensor Networks*. [S.l.], 2005. p. 364–369.

[2] GOYAL, D.; TRIPATHY, M. R. Routing protocols in wireless sensor networks: a survey. In: IEEE. *2012 Second International Conference on Advanced Computing & Communication Technologies (ACCT)*. [S.l.], 2012. p. 474–480.

[3] MADUREIRA, H. M. G. et al. System-level power consumption modeling of a SoC for WSN applications. In: IEEE. *IEEE 2nd International Conference on Networked Embedded Systems for Enterprise Applications (NESEA)*. [S.l.], 2011. p. 1–6.

[4] DELTIMPLE, N. et al. Design of class E power VCO in 65nm CMOS technology: Application to RF transmitter architecture. In: IEEE. *IEEE International Symposium on Circuits and Systems, 2008.* [S.l.], 2008. p. 984–987.

[5] SJOLAND, H.; KARIMI-SANJAANI, A.; ABIDI, A. A. A merged CMOS LNA and mixer for a WCDMA receiver. *IEEE Journal of Solid-State Circuits*, IEEE, v. 38, n. 6, p. 1045–1050, 2003.

[6] KOUCHAKI, M. et al. Down-conversion self-oscillating mixer by using CMOS technology. In: IEEE. *2012 IEEE 8th International Colloquium on Signal Processing and its Applications (CSPA)*. [S.l.], 2012. p. 33–36.

[7] ETSI, T. *LTE; Evolved Universal Terrestrial Radio Access (E-ULTRA); User Equipment (UE) Radio Transmission and Reception (3GPP TS 36.101 V11.2.0 Release 11)*. [S.l.]: LTE.

[8] NOTE, A. A. 3gpp long term evolution: System overview, product development, and test challenges. *Literature Number*, 2009.

[9] RAZAVI, B. *RF Microelectronics*. [S.l.]: Prentice Hall New Jersey, 1998.

[10] LOKE, A.; ALI, F. Direct conversion radio for digital mobile phones-design issues, status, and trends. *IEEE Transactions on Microwave Theory and Techniques*, IEEE, v. 50, n. 11, p. 2422–2435, 2002.

[11] RAZAVI, B. Design considerations for direct-conversion receivers. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, IEEE, v. 44, n. 6, p. 428–435, 1997.

[12] REARWIN, R. H.; COLLINS, F. P. *FM Heterodyne Transmitter*. jan. 29 1974. US Patent 3,789,302.

[13] MUHAMMAD, K.; STASZEWSKI, R. B.; LEIPOLD, D. Digital RF processing: Toward low-cost reconfigurable radios. *IEEE Communications Magazine*, IEEE, v. 43, n. 8, p. 105, 2005.

[14] CHI, B. et al. A 65 nm CMOS fully-integrated dynamic reconfigurable differential power amplifier with high gain in both bands. *Microelectronics Journal*, Elsevier, v. 42, n. 6, p. 855–862, 2011.

[15] BASCHIROTTO, A. et al. Baseband analog front-end and digital back-end for reconfigurable multi-standard terminals. *IEEE Circuits and Systems Magazine*, IEEE, v. 6, n. 1, p. 8–28, 2006.

[16] RAWAT, K.; HASHMI, M. S.; GHANNOUCHI, F. M. Dual-band RF circuits and components for multi-standard software defined radios. *IEEE Circuits and Systems Magazine*, IEEE, v. 12, n. 1, p. 12–32, 2012.

[17] DELTIMPLE, N. *Etude et Réalisation d'un Amplificateur de Puissance Reconfigurable en Technologie BiCMOS SiGe pour des Applications Multi-Standards GSM/DCS/UMTS*. Tese (Doutorado) — Université Sciences et Technologies-Bordeaux I, 2005.

[18] MOHAMMADI, A.; GHANNOUCHI, F. M. RF power amplifier and linearization techniques. In: *RF Transceiver Design for MIMO Wireless Communications*. [S.l.]: Springer, 2012. p. 77–128.

[19] CRIPPS, S. C. *Advanced Techniques in RF Power Amplifier Design*. [S.l.]: Artech House, 2002.

[20] ROGERS, J. W.; PLETT, C. *Radio Frequency Integrated Circuit Design*. [S.l.]: Artech House, 2014.

[21] CARNEIRO, M. L. *Design, Optimization and Integration of Doherty Power Amplifier for 3G/4G Mobile Communications*. Tese (Doutorado) — Université Sciences et Technologies-Bordeaux I, 2013.

[22] WONG, S. L.; LUO, S. A 2.7-5.5 v, 0.2-1 w biCMOS RF driver amplifier IC with closed-loop power control and biasing functions. *IEEE Journal of Solid-State Circuits*, IEEE, v. 33, n. 12, p. 2259–2264, 1998.

[23] KIM, B. et al. The doherty power amplifier. *IEEE Microwave Magazine*, IEEE, v. 7, n. 5, p. 42–50, 2006.

[24] LEE, T. H. *The Design of CMOS Radio-Frequency Integrated Circuits*. [S.l.]: Cambridge university press, 2004.

[25] CRIPPS, S. C. *RF Power Amplifiers for Wireless Communications*. [S.l.]: Artech House Norwood, 2006.

[26] JOHNSON, T.; SOBOT, R.; STAPLETON, S. Cmos RF class D power amplifier with bandpass sigma-delta modulation. *Microelectronics journal*, Elsevier, v. 38, n. 3, p. 439–446, 2007.

[27] REYNAERT, P.; STEYAERT, M. Analysis and design of the class E power amplifier in CMOS. In: *RF Power Amplifiers for Mobile Communications*. [S.l.]: Springer, 2006. p. 65–110.

[28] TELEGDY, A.; MOLNAR, B.; SOKAL, N. O. Class - Em switching-mode tuned power amplifier-high efficiency with slow-switching transistor. *IEEE Transactions on Microwave Theory and Techniques*, IEEE, v. 51, n. 6, p. 1662–1676, 2003.

[29] SOKAL, N. O.; SOKAL, A. D. Class E - a new class of high-efficiency tuned single-ended switching power amplifiers. *IEEE Journal of Solid-State Circuits*, IEEE, v. 10, n. 3, p. 168–176, 1975.

[30] SEKIYA, H.; EZAWA, T.; TANJI, Y. Design procedure for class E switching circuits allowing implicit circuit equations. *IEEE Transactions on Circuits and Systems I: Regular Papers*, IEEE, v. 55, n. 11, p. 3688–3696, 2008.

[31] WEI, M.-D. et al. Investigation of wideband load transformation networks for class E switching-mode power amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, IEEE, v. 60, n. 6, p. 1916–1927, 2012.

[32] MAZZANTI, A. et al. Analysis of reliability and power efficiency in cascode class E pas. *IEEE Journal of Solid-State Circuits*, IEEE, v. 41, n. 5, p. 1222–1229, 2006.

[33] CHIRONI, V. et al. A digitally modulated class E polar amplifier in 90 nm CMOS. *IEEE Transactions on Circuits and Systems I: Regular Papers*, IEEE, v. 60, n. 4, p. 918–925, 2013.

[34] CHAKRABARTI, A.; KRISHNASWAMY, H. An improved analysis and design methodology for RF class E power amplifiers with finite DC-feed inductance and switch on-resistance. In: IEEE. *2012 IEEE International Symposium on Circuits and Systems (ISCAS)*. [S.l.], 2012. p. 1763–1766.

[35] SONG, Y. et al. A cmos class E power amplifier with voltage stress relief and enhanced efficiency. *IEEE Transactions on Microwave Theory and Techniques*, IEEE, v. 58, n. 2, p. 310–317, 2010.

[36] LEE, O. et al. A charging acceleration technique for highly efficient cascode class E CMOS power amplifiers. *IEEE Journal of Solid-State Circuits*, IEEE, v. 45, n. 10, p. 2184–2197, 2010.

[37] KAZIMIERCZUK, M. K. et al. Class E mosfet tuned power oscillator design procedure. *IEEE Transactions on Circuits and Systems I: Regular Papers*, IEEE, v. 52, n. 6, p. 1138–1147, 2005.

[38] OZEN, M.; JOS, R.; FAGER, C. Continuous class E power amplifier modes. *IEEE Transactions on Circuits and Systems II: Express Briefs*, IEEE, v. 59, n. 11, p. 731–735, 2012.

[39] ALLAN, A. et al. 2001 technology roadmap for semiconductors. *Computer*, IEEE, v. 35, n. 1, p. 42–53, 2002.

[40] TAN, J.; HENG, C.-H.; LIAN, Y. Design of efficient class E power amplifiers for short-distance communications. *IEEE Transactions on Circuits and Systems I: Regular Papers*, IEEE, v. 59, n. 10, p. 2210–2220, 2012.

[41] TIEBOUT, M. A 480 μw 2 ghz ultra low power dual-modulus prescaler in 0.25 μm standard CMOS. In: IEEE. *IEEE International Symposium on Circuits and Systems (ISCAS)*. [S.l.], 2000. v. 5, p. 741–744.

[42] WANG, J.; LIU, Z. A merged up-conversion mixer-VCO based on current reuse. In: IEEE. *IEEE Subthreshold Microelectronics Conference (SubVT)*. [S.l.], 2012. p. 1–3.

[43] CHENG, K.-W.; NATARAJAN, K.; ALLSTOT, D. J. A ccurrent reuse quadrature GPS receiver in 0.13um CMOS. *IEEE Journal of Solid-State Circuits*, IEEE, v. 45, n. 3, p. 510–523, 2010.

[44] GONZALEZ, G. *Foundations of Oscillator Circuit Design*. [S.l.]: Artech House, 2007.

[45] EBERT, J.; KAZIMIERCZUK, M. Class E high-efficiency tuned power oscillator. *IEEE Journal of Solid-State Circuits*, IEEE, v. 16, n. 2, p. 62–66, 1981.

[46] SEKIYA, H.; JIANMING, L.; YAHAGI, T. Novel design procedure for mosfet class E oscillator. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, The Institute of Electronics, Information and Communication Engineers, v. 87, n. 9, p. 2241–2247, 2004.

[47] JEON, S.; SUAREZ, A.; RUTLEDGE, D. B. Nonlinear design technique for high-power switching-mode oscillators. *IEEE Transactions on Microwave Theory and Techniques*, IEEE, v. 54, n. 10, p. 3630–3640, 2006.

[48] GITSEVICH, A.; KIRKPATRICK, D.; JR, L. D. Solid-state high power RF oscillator. In: IEEE. *2001 IEEE MTT-S International Microwave Symposium Digest*. [S.l.], 2001. v. 3, p. 1423–1426.

[49] DEVINE, R.; TOFIGHI, M.-R. Class E colpitts oscillator for low power wireless applications. *Electronics Letters*, IET, v. 44, n. 21, p. 1257–1258, 2008.

[50] LIN, C.-H.; LI, W.-P.; CHANG, H.-Y. A fully iitegrated 2.4 GHz 0.5 W high efficiency class E voltage controlled oscillator in 0.15um PHEMT process. In: *Microwave Conference Proceedings (APMC), 2011 Asia-Pacific*. [S.l.: s.n.], 2011. p. 864–867.

[51] CHEE, Y. H.; NIKNEJAD, A. M.; RABAEY, J. M. An ultra-low-power injection locked transmitter for wireless sensor networks. *IEEE Journal of Solid-State Circuits*, IEEE, v. 41, n. 8, p. 1740–1748, 2006.

[52] KLYMYSHYN, D. M.; KUMAR, S.; MOHAMMADI, A. Direct GMSK modulation with a phase-locked power oscillator. *IEEE Transactions on Vehicular Technology*, IEEE, v. 48, n. 5, p. 1616–1625, 1999.

[53] GHANNOUCHI, F. M.; HAMMI, O. Behavioral modeling and predistortion. *IEEE Microwave Magazine*, IEEE, v. 10, n. 7, p. 52–64, 2009.

[54] LAKI, B. D.; KIKKERT, C. J. Adaptive digital predistortion for wideband high crest factor applications based on the WACP optimization objective: A conceptual overview. *IEEE Transactions on Broadcasting*, IEEE, v. 58, n. 4, p. 609–618, 2012.

[55] HUSSEIN, M. A. et al. Digital predistortion for RF power amplifiers: State of the art and advanced approaches. In: *11th IEEE International NEWCAS Conference*. [S.l.: s.n.], 2013. p. NEWCAS–2013.

[56] REYNAERT, P.; STEYAERT, M. *RF Power Amplifiers for Mobile Communications*. [S.l.]: Springer Science & Business Media, 2006.

[57] MCCUNE, E. Envelope tracking or polar - which is it?[microwave bytes]. *IEEE Microwave Magazine*, IEEE, v. 13, n. 4, p. 34–56, 2012.

[58] CHOU, J. Reducing the design complexity of next-generation handsets. *RF DESIGN*, CARDIFF PUBLISHING COMPANY INC, v. 29, n. 9, p. 28, 2006.

[59] MCCUNE, E. Polar modulation and bipolar RF power devices. In: *IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*. [S.l.: s.n.], 2005.

[60] WATKINSON, S. W. *Polar Loop Transmitter*. [S.l.]: Google Patents, dez. 16 1986. US Patent 4,630,315.

[61] CHADWICK, P. E. *Polar Loop Transmitter*. [S.l.]: Google Patents, jan. 18 2005. US Patent 6,844,788.

[62] REDOUTÉ, J.-M.; STEYAERT, M. *EMC of Analog Integrated Circuits*. [S.l.]: Springer Science & Business Media, 2009.

[63] KIM, B. C. Novel design of carbon nanotube based RF inductors. *Journal of Nanotechnology in Engineering and Medicine*, American Society of Mechanical Engineers, v. 1, n. 1, p. 011003, 2010.

[64] NIKNEJAD, A. M. *Electromagnetics for High-Speed Analog and Digital Communication Circuits*. [S.l.]: Cambridge University Press, 2007.

[65] JACKSON, J. D.; JACKSON, J. D. *Classical Electrodynamics*. [S.l.]: Wiley New York etc., 1962.

[66] RAMO, S.; WHINNERY, J. R.; DUZER, T. V. *Fields and Waves in Communication Electronics*. [S.l.]: John Wiley & Sons, 2007.

[67] POZAR, D. M. *Microwave Engineering*. [S.l.]: John Wiley & Sons, 2009.

[68] NIKNEJAD, A. M.; MEYER, R. G. Analysis of eddy-current losses over conductive substrates with-aapplications to monolithic inductors and transformers. *IEEE Transactions on Microwave Theory and Techniques*, Citeseer, v. 49, n. 1, p. 166–176, 2001.

[69] BELOT, D. et al. *Circuit Électronique de Fourniture d'un Signal Oscillant (Power VCO Classe E)*. [S.l.]: Institut National de la Propriété Industrielle, 2009.

[70] SOKAL, N. O. Class E RF power amplifiers. *QEX Commun. Quart*, v. 204, p. 9–20, 2001.

[71] INICIATIVE, G. G. *Evolved Universal Terrestrial Radio Access (E-ULTRA) User Equipment (UE) Rradio Transmission and Reception*. [S.l.]: Release 11, 2012.

[72] LATHI, B. P. *Modern Digital and Analog Communication Systems*. [S.l.]: Oxford University Press, Inc., 1990.

[73] SAMORI, C.; LEVANTINO, S.; LACAITA, A. L. Integrated LC oscillators for ffrequency synthesis in wireless applications. *IEEE Communications Magazine*, IEEE, v. 40, n. 5, p. 166–171, 2002.

[74] CHANG, H.-Y.; WU, Y.-S.; WANG, Y.-C. A 38% tuning bandwidth low phase noise differential voltage controlled oscillator using a 0.5 um e/d-PHEMT process. *IEEE Microwave and Wireless Components Letters*, IEEE, v. 19, n. 7, p. 467–469, 2009.

[75] BESERRA, G. S. et al. System-level modeling of a reconfigurable system on chip for wireless sensor networks applications. In: IEEE. *2010 International Conference on Intelligent and Advanced Systems (ICIAS)*. [S.l.], 2010. p. 1–5.